Application Note

AN-4710

Operating Manual

iDDS Frequency Synthesizer

Isomet Software Version: v3.04 – V3.08

This guide with the aid of the Isomet Windows software will allow the user to control the iDDS and generate single frequencies, frequency ramps or pre-loaded sequence(s) of frequencies.

Common basic connections are given in Appendix A
A full list of model specific pin connections is supplied with the iDDS test data sheet.

For users wishing to develop their own operating software, a full list of software instructions is given in Appendix D and DDS register listing in Appendix B

A typical set-up with amplifier and AO deflector is given in Appendix C

Variants

MODEL						
iDDS -	**X**	**Y**	**-**	**Z**		
Outputs					Comms (J1)	Control (J2)
Single	**1**			**U**	USB	TTL Compatible IO signals
Dual	**2**			**SE**	RS232	TTL Compatible IO signals
Custom options				**D**	RS485	Differential logic IO signals
Frequency Doubled		**F**				
Parallel input frequency select		**P**				
Voltage control frequency tune		**A**				

e.g.

iDDS-2-U — Dual output. Single ended TTL compatible Input Control Signals (J2). USB 1.1 Comms Input (J1)

iDDS-1F-SE — Frequency Doubled single output. Single ended TTL compatible Input Control Signals (J2). RS232 Comms Input (J1), 115Kbaud
(Refer Freq x 2 Addendum pg58)

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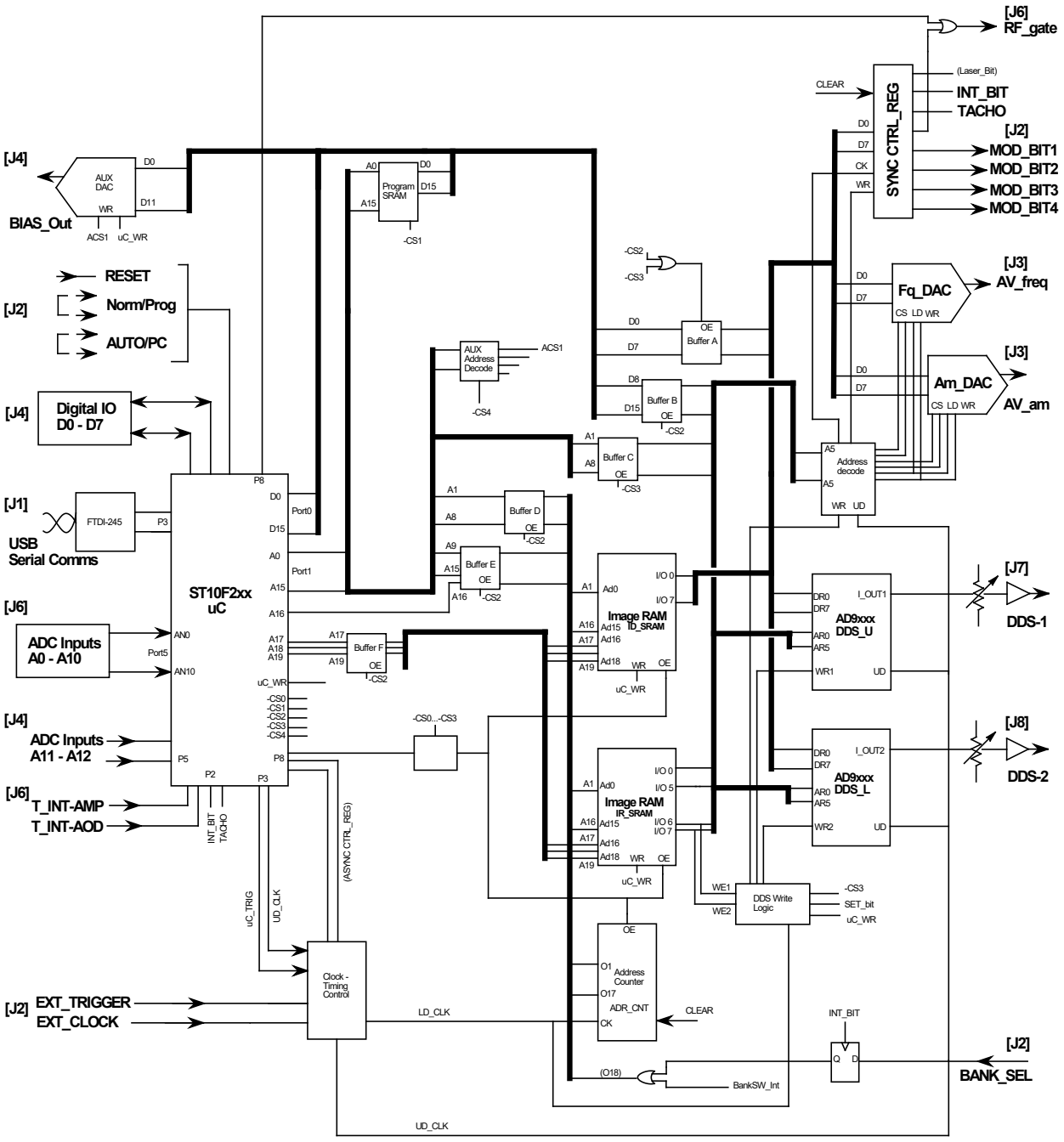


iDDS-2 Block diagram
Connector idents shown [J]

Overview

There are four basic operating modes, summarized below.
Sections 2 - 4 describe operation using the Isomet GUI Software
Sections 5 - 9 describe general programming and operating procedures

Summary

- Internal iDDS operating code.

The operating features of the iDDS are defined by the hardware configuration and control code installed at the time of manufacture.

Most of the typical features are described in this manual. Customized units will be supplied with additional application notes.

Typical code versions are:

v77w3S *Standard functions*
v77w3A *Voltage control of the output frequency (Pseudo VCO mode)*
v77w3P *8bit parallel input selects 1 of 256 pre-defined output frequencies*
v77w3L *Internal memory configured to give 64 pages of 290 frequency profiles*

[To query the installed code, input **'=v'** in the *Serial I/O Data* window of the MAIN menu
The iDDS will respond with **@v77w3** or similar. (Refer section 1).]

- Single Tone or *DIRECT* Mode (section 2)

Typical applications: Frequency shifting, AO deflector "manual" tuning of scan position, AO tuneable filter "manual" tuning of selected filter pass wavelength.

The DDS chips are addressed directly from the Host PC or via a boot-up routine.
Each output of the dual version, iDDS-2 can be set independently.
Available Functions:

- Single tone (static frequency) output.
- Zero to Max Amplitude control.
- 0-360deg Phase shift between outputs for the iDDS-2
- Differential frequency offset between the outputs for the iDDS-2

Frequency tuning response is limited by the USB or RS232 data rate and the desired data resolution.

- *CHIRP* Mode (section 3)

Typical application: Fast linear AO deflector scanning

The DDS chips are addressed directly from the Host PC or via a boot-up routine.
A chirp is generated by rapidly incrementing the frequency. The increment step value and dwell time per increment are user programmable. Available Functions:

- Frequency Chirp (or Sweep), Up or Down
  Plus
- Set value or ramping amplitude control
- Set value Phase shift

The Chirp mode offers the fastest frequency sweep capability, with a minimum dwell time of 6.7nsec per frequency increment.
In this fastest mode, phase and amplitude settings remain constant across the sweep.

Once programmed, a single trigger input is all that is required to initiate a defined frequency sweep. A further input level defines the sweep direction.

The sweep parameters can be programmed into non-volatile memory.

- *IMAGE* Mode (section 4)

Typical applications:
- User defined, repeating or random pattern generation for AO scanning or AO filtering.
- Active acoustic Beam steering using Phase control.

The DDS chips are controlled via internal SRAM and look-up tables (LUT's). These are programmed from the Host PC or via a custom boot-up routine. Data is stored in sets. Each set comprises of Frequency, Amplitude, Phase and Ancillary control data. When outputting, each location of the internal memory is addressed in sequence. The RF signal responds to the current data set following a valid clock input. This update clock rate is under user control.

Any frequency profile can be down loaded including uni-directional and bi-directional frequency sweeps. The key advantage of this mode is that specific amplitude and/or phase value can be assigned to each frequency. This permits power vs. frequency programming plus phase steering of the RF outputs.

This mode is the most flexible and allows a high data throughput when applying frequency specific amplitude (and phase) control. The minimum dwell time per frequency point is less than 1usec.

Once the iDDS is programmed, the user applied trigger and clock inputs control the data output rate. This allows synchronization with external systems

- *DataQ* Mode (section 5)

Typical applications
- Dynamic differential frequency shifting.
- Complex frequency phase /amplitude sequencing.

Similar to the Image mode above, except the data is written directly into the SRAM, storage without any adaptation by the look-up tables (LUT's). This mode differs in that unique and independent frequency, phase and amplitude data can be written to each output of the dual iDDS-2. The full resolution of the DDS chips can be exploited.

Once the iDDS is programmed, the user applied trigger and clock inputs control the data output rate. This allows synchronization with external systems

1.0 Operation using the Isomet GUI Software

For USB versions load the FTDI drivers before installing the Isomet GUI software.

For USB versions for Windows XP and Vista

The iDDS-x-U utilizes the FTDI245R USB-parallel chip.
This version offers true USB interface and maintains the original RS232 interface for backwards compatibility. Note: Both interfaces should not be used at the same time.

An interface cable is supplied. This is NOT an RS232 to USB inline converter. It serves only as a connector adaptor to route the USB signals onto unused pins of an existing 9 way connector J3.

The FTDI DLL and VCP driver files are included on the CDROM supplied with the iDDS.
They can also be downloaded from: www.ftdichip.com/drivers/d2xx.htm

The iDDS USB port supports the following data rates depending on the transfer method:

VCP : 300Kbytes/sec
DLL : up to 12Mbits/sec

This compares to 115Kbaud for the RS232 connection.

The Isomet GUI software uses VCP (virtual comms port) for simple commands and a DLL routine for large file downloads.

Software Installation

BEFORE connecting the iDDS-x to the USB port install the USB drivers.
Browse to the USB driver folder on the CDROM supplied with the iDDS.

Run: *CDM2.04.16.exe*

(You may need to allow Administrator privileges)

After the drivers are installed onto the host PC, power up and plug in the iDDS-x.

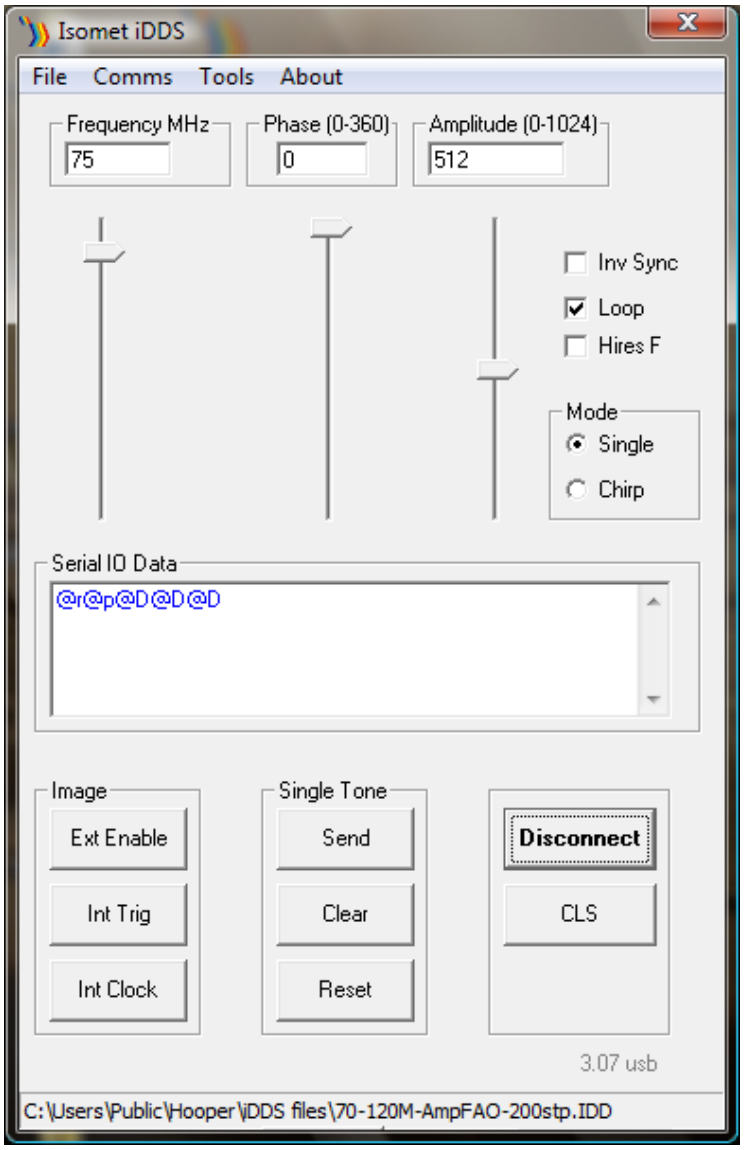
For both RS232 and USB versions

Install the Isomet iDDS Software onto the host PC with a free Serial / USB port and running Win XP or Vista. See the Readme file on the installation CD for guidance.

Connect the Comms and DC power (see Basic Connection Section below)

Run the software by clicking on the Isomet logo on the Desktop.
(For Vista, you may need to 'Run as Administrator' and "Allow")

There are two main windows. The first is similar to below.



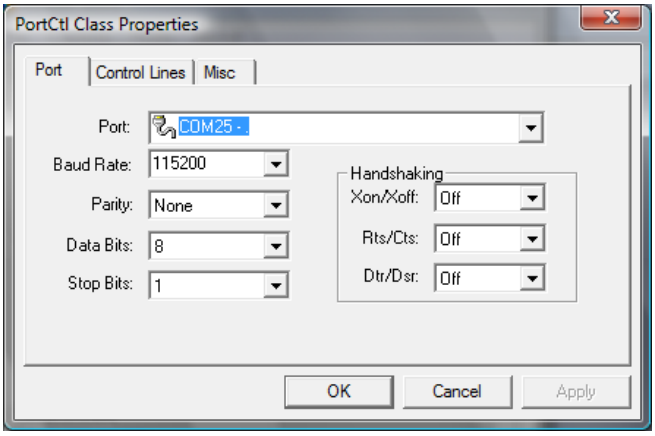
1.1 MAIN Menu:

The ***Clear*** button places the DDS into a known state and should be applied between mode changes. It does not reset the internal micro-controller (uC).

The ***Reset*** is equivalent to applying a hardware Reset. This will reset the uC.

1,2 Communication

Select the ***CommPort*** pull down menu and check the Port and Baud rate suit the serial port of the iDDS as specified and supplied.



Normal settings:

Serial Port versions

RS232: Com1 115Kbaud.
The iDDS will be supplied for either RS232 or RS485, not both. The Baud rate is fixed.

USB Port versions

USB: The Isomet GUI software uses VCP for simple commands (DLL routine for large file downloads). Select the appropriate COM port assigned by the PC for VCP. Typically Com 3 or higher.

Click the ***Connect*** button. (Changes to ***Disconnect***)

The iDDS should respond and send **@r@p@D** characters to the Serial I/O Data window.

Note for USB versions
On first power up or following a RESET, the initial response characters transmitted from the iDDS may be missing. This is due to the reset cycle time of the iDDS USB port.

2.0 Single Tone

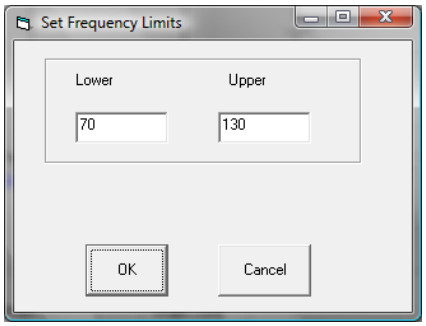
From the MAIN menu (***Single Mode*** Button Checked), the iDDS can be commanded to output a fixed frequency at given Amplitude and Phase. Phase only applies to the iDDS-2, where a phase difference is applied between the two outputs J7 and J8.

Numbers can be entered directly into the boxes, or by means of the slider controls using the mouse or Up/Down arrow keys.

Click the ***Send*** button to initiate the Single Tone Mode.

2.1 Slider Limits

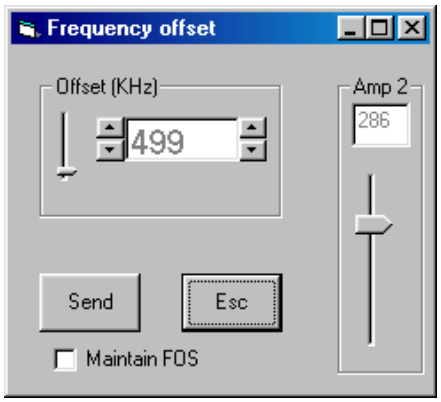
The Frequency slider control limits can be customized
Select the ***Tools*** pull down menu and click on ***F Limits***



Enter the desired end points and click OK

2.2 Frequency Differential

Where a frequency difference is required between the two outputs of the iDDS-2 series, select the ***Tools*** pull down menu and click on ***Frequency Offset.***



Offset range is 0 to 5000 KHz in 0.1KHz step resolution

Select the slider with the mouse or use the Up/Down Arrow keys to increment/decrement values.

The Frequency Offset is applied to output RF2 (J8).
In addition the amplitude of this output is independently set when the Frequency Offset is enabled (***Amp2***). Normally this value is set to the same value as the Amplitude slider in the MAIN menu.

Hit the SEND button to load the offset values.

Check the ***Maintain FOS*** box to keep the displayed offsets when returning to the MAIN (Single Tone) menu. The warning **'FOS'** will appear to signify that the offset is in force.

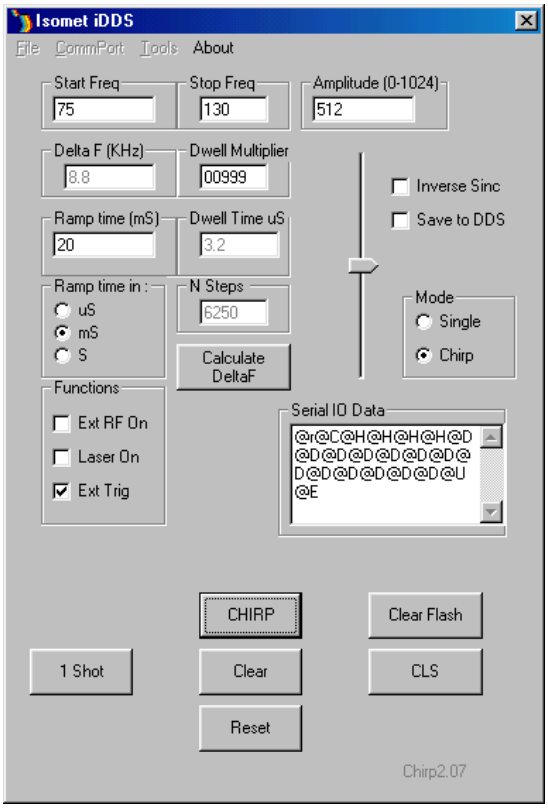
Any subsequent changes in Frequency from the MAIN menu will be applied to output RF1 (J7) and the same Frequency value plus the Offset Value will be applied to RF2 (J8).
Note: the Offset is not applied if RF1 frequency reaches the upper limit (See 'Slider Limits')

To remove the FOS function:

Select the ***Tools*** pull down menu and click on ***Frequency Offset.***
Uncheck the ***Maintain FOS*** box. Return to the MAIN menu and hit SEND.
Both outputs will now be at the same frequency. The warning **'FOS'** will disappear.

3.0 Frequency Chirp (Ramp) Menu

Highlighting the ***Chirp Mode*** Button changes the window to the Chirp menu.



The user can specify the Start and desired Stop Frequency, the Ramp duration and the Dwell Multiplier. The ramp scale factor (microseconds, milliseconds or seconds) is selected by the radio buttons

The dwell time per frequency increment is given by: t_{dwell} = (Dwell multiplier +1) x 3.2nsec. This figure is displayed according to the dwell time input by the user.

The number of frequency steps N or increments is then calculated from:

N = Ramp Duration / t_{dwell}……and rounded down

Click the ***Calculate DeltaF*** button to view result.

The Stop frequency is automatically readjusted if necessary to accommodate the integer value N

An error message will be displayed if the ***Delta F*** value is less than the internal frequency resolution of the DDS (18.6Hz). Increase the ***Dwell Multiplier*** (also referred to as RAMP Rate Clock) to correct.

Click the ***Chirp*** button to load data to the iDDS.

To initiate a frequency ramp:

- With the ***Ext Trig*** box unchecked, click the ***1 Shot*** button once per ramp start.
- With the ***Ext Trig*** box checked, an external Trig input is required on J2.

This external trigger signal must be a positive going pulse of > 500nsec duration.

The iDDS is initiated on the positive edge of the pulse and the ramp start is coincident with the negative edge. The output will ramp in frequency for the duration specified. At the end of the desired period, the frequency will park at the Stop value until the next trigger input. (Or Start value for High to Low Frequency Chirp). See diagram below. The trigger pulse width can be considered equivalent to a VCO 'fly back' time

The DDS can generate up or down ramps according to the Direction (Bank select) switch input on J2, pin 3/15:

Low = Low to high frequency
High (or open circuit) = High to Low frequency

External Trigger Input Timing Spec:

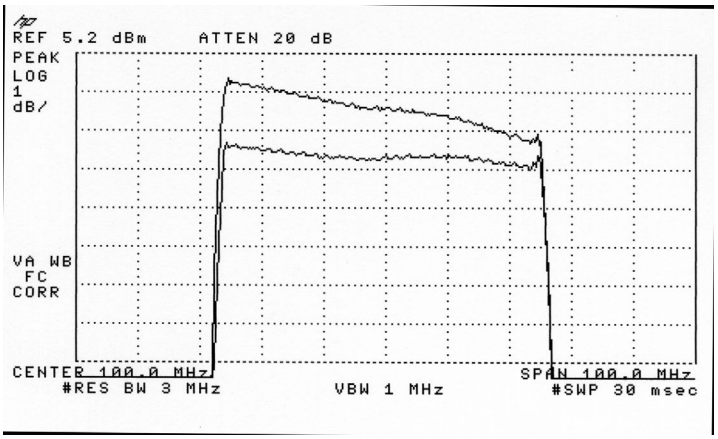
Minimum pulse width t_h : 0.5usec
Minimum repetition rate t_l : equal or greater than the desired ramp duration t_{rp}

The internal DDS chips include an Inverse Sinc filter function to flatten the amplitude vs. frequency response.

With ***Inverse Sinc*** filter box unchecked, the droop in amplitude from low to high frequency is in the order of 1.0dB.

With ***Inverse Sinc*** filter box checked, the amplitude variation from low to high frequency is less than 0.5dB. However the 5V DC current draw increases significantly (2.7A to 3.5A for the dual output iDDS-2), with a corresponding increase in thermal dissipation.
Use this option only if required and ensure adequate free circulation of air around the iDDS to aid cooling.

Typical 75-125MHz Frequency response with the filter ON (lower trace) and OFF (upper trace). Vertical scale 1dB / div.



For the Dual output iDDS-2 series, both outputs will chirp with a nominal 0 deg phase shift between the outputs.

The additional Check boxes provide static output signals on J2 (**Laser On**) and J6 (**Ext RF On**).

3.1 Saving Chirp Settings

The chirp settings can be stored in Non-volatile FLASH memory in the iDDS.
First clear the Flash sector by clicking the ***Clear Flash*** button. The iDDS will respond with **'@b'** (If a 'Clear' is not initiated, instructions are appended onto any existing data in Flash).

Save new instructions by checking the ***Save Settings to DDS*** box and clicking the ***Chirp*** button. A series of '**@a**' character pairs will be seen in the Serial I/O Data window. On completion, the ***Save Settings to DDS box*** will self un-check.

With data successfully loaded in FLASH memory the iDDS can operate autonomously from the Host PC by configuring the iDDS to run Stand-alone.

3.2 Running Stand-alone

Make the 'Auto' switch / link on J2 and the cycle the DC power or ***Reset***

At this point, the PC serial port can be disconnected. However if the PC serial connection is left in place, then the series of boot instructions from Flash to uC will be echoed to the PC and visible in the Serial I/O Data window.

The iDDS will boot up in the programmed chirp mode and output the desired frequency profile for every trigger input. The ramp direction is set according to the Direction (Bank select) Switch Input on J2.

To re-initiate PC communication, open the 'PC' switch / link on J2 and cycle the DC power or ***Reset*** .

4.0 Image Mode

A user defined sequence of Frequency, Amplitude and Phase values can be clocked from internal memory. (Phase control applies to Beam steered AO deflectors.)

This method can be used to generate almost any pattern form a simple line scan with uniform intensity to a completely random set of frequencies and amplitudes.

A frequency 'image' of up to 18K points is stored in a 131K x 8bit Static RAM blocks within the iDDS. Images are loaded via the ***File*** pull down menu and must have the extension *.idd.

The Image data also includes a user settable control byte for each frequency entry.
See page 34, **Synchronous Control register SYCRL_REG**

[An optional large memory version of the iDDS with 512K x 8bit SRAM's can store up to 2 frequency 'images' of 36K points each or a single frequency image of up to 64K points.
A 'Bank_Switch' signal connected to the MSB address bit of the SRAM, selects the start point for the two Image configurations. This is software and hardware controllable (via J2)].

Once the Image is loaded, the RAM address bus is switched from the internal uC to fast autonomous address counters. These address counters increment according to the logic of clock and trigger control signals (Ext_Clock / Ext_Trigger or Int Clk / 1 Shot). Each clock will produce a new frequency profile at the *iDDS* output(s)

The typical maximum data rate in this mode is 1MHz (i.e. 1usec per new frequency point)

Two files are required:

- The ***.IDD** file contains Frequency, Amplitude and Control data ('=L' Output Word)
- The ***.CAL** file contains the calibration Phase and Amplitude data for each frequency point. ('=F' Output Word). This defaults to a Phase of 000 and Amplitude of FFF for most single output iDDS-1 versions, where the phase data is not relevant. Nevertheless this table still needs to be loaded.

Both files contain amplitude data. The two amplitude values are multiplied together in the iDDS. The amplitude data in the Data file allows for intensity modulation without the need for modifying the calibration LUT.

The LUT calibration data (*.CAL) resides in non-volatile FLASH memory and will not be lost during power down or reset.

The Image data (*.IDD) is stored in SRAM and will requiring reloading after a power down or reset.

In total there are three steps to inputting an Image File:

Load: Look up table. (*.CAL file)
Load: Image file. (*. IDD file)
Load: Headers. (=Hnn command)

These are described in detail below.

Data Flow

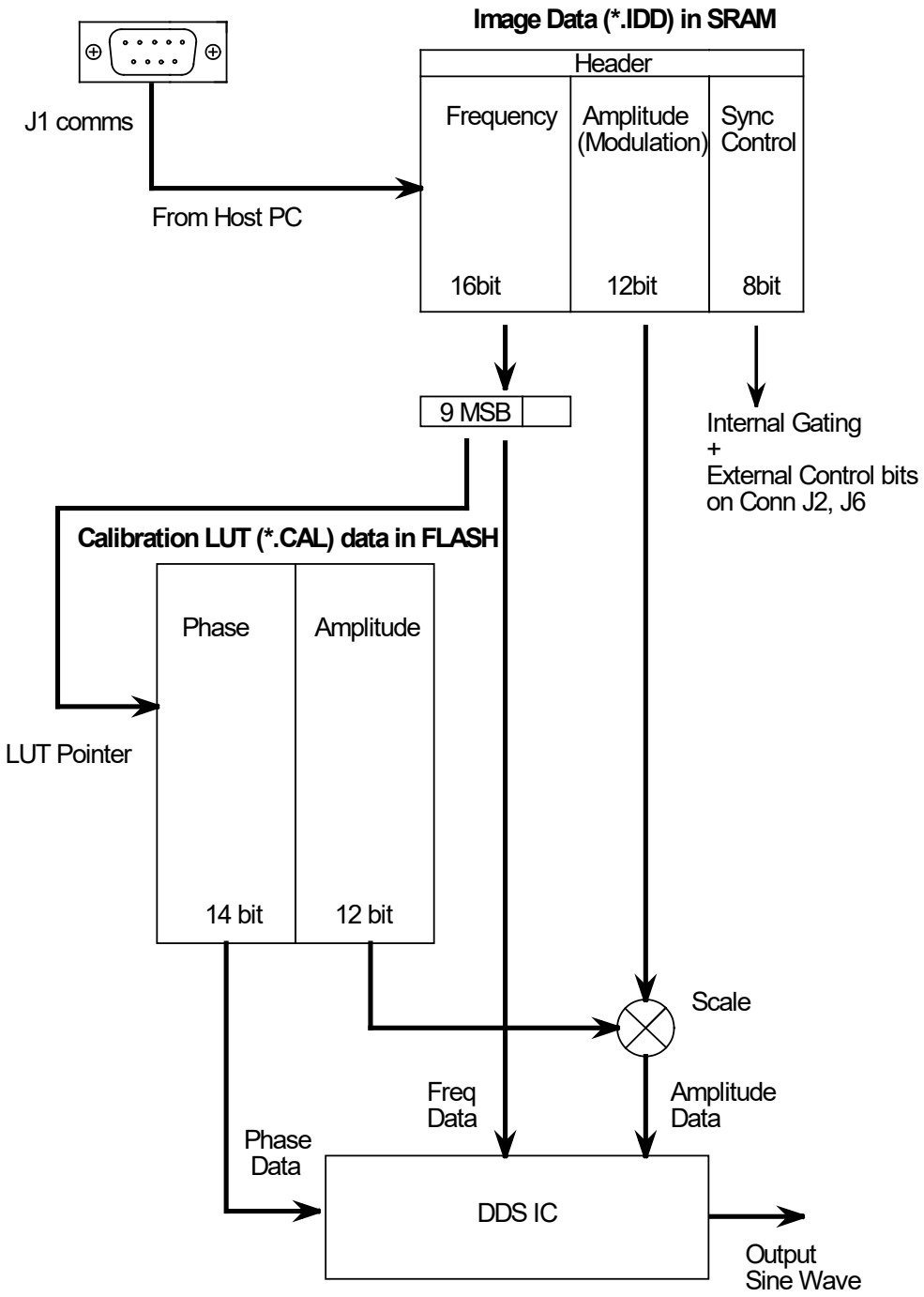


Image Data (*.IDD) in SRAM
Header
Frequency
Amplitude (Modulation)
Sync Control
16bit
12bit
8bit
J1 comms
From Host PC
9 MSB
Internal Gating
+
External Control bits
on Conn J2, J6
Calibration LUT (*.CAL) data in FLASH
Phase
Amplitude
14 bit
12 bit
LUT Pointer
Scale
Freq Data
Amplitude Data
Phase Data
DDS IC
Output Sine Wave

.

4.1 Calibration Look-up Table (LUT)

Each Image point is defined by a 16-bit frequency, 12-bit amplitude and 8 bits of control data. A predetermined phase shift is programmed into one of the two DDS IC's. The 14 bit Phase/Amp data is 'fetched' on the fly during the image load into SRAM, using the 9MSB's of the frequency value as a pointer to the FLASH memory location. A valid LUT must be installed prior to an Image load into memory.

This value is frequency dependant and is stored in a Look-up-table (LUT) within a segment of the Flash memory.

Two calibration Look-up-tables are provided.

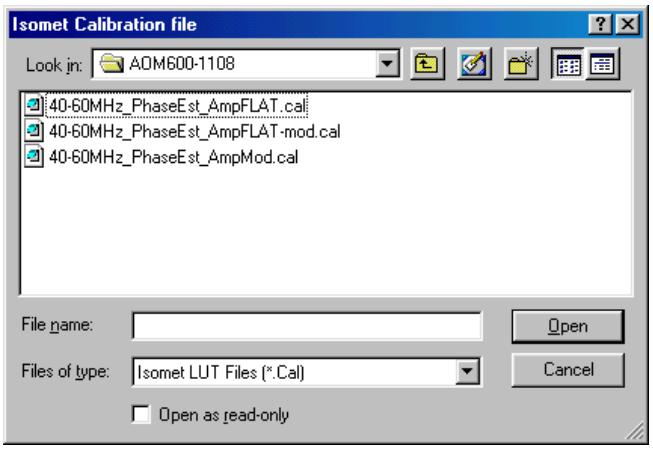
- One is a template with maximum amplitude, zero phase for all entries.
- Second is an estimated table with values appropriate to the AO device supplied with the iDDS.

Optimum performance requires the LUT values to be determined and optimized with the AO device operating in the specific system or application.

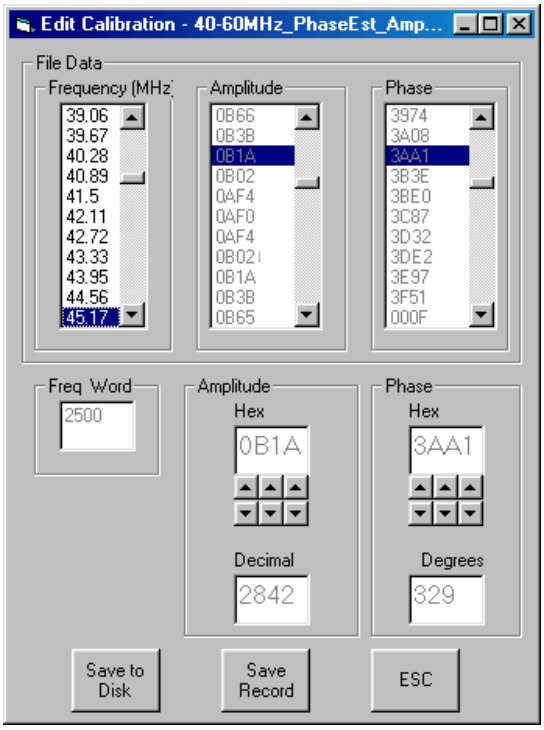
Note: Should the mechanical Bragg angle or the laser beam input angle be adjusted then it will be necessary to repeat the calibration procedure. This is especially true for Beam steered AO deflectors

To edit / generate a LUT, select the ***Tools*** pull down menu, click on ***Edit LUT***

Select the *.cal file to be edited.



This will be loaded and the following window is presented:



Scroll to the desired Frequency. The corresponding Amplitude and Phase values are addressed.

Use the Up-Down ***Arrow*** buttons below the “Hex” windows to tune the Amplitude and/or Phase values.

The iDDS will update its output on each change.

Measure the first order diffracted power from the AO device and adjust the phase and amplitude to maximise the intensity.

Start by adjusting the phase at a low RF amplitude setting. Once the optimum phase has been determined, THEN adjust the RF amplitude to set the first order intensity at the desired level for uniformity.

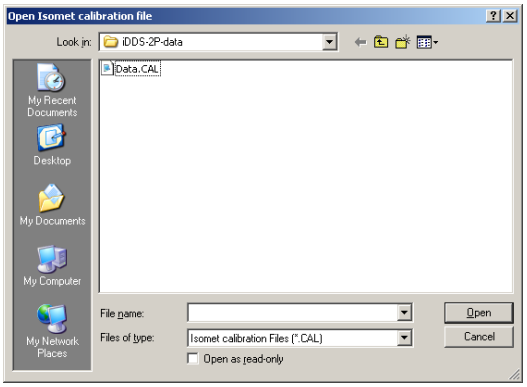
Once editing is complete for that record, click on ***Save Record*** to update the new values in the LUT BEFORE proceeding to the next frequency.

One all edits are complete click ***Save to Disk*** to permanently save the changed values to a new existing file.

4.2 Loading Files : Data and Calibration

The Calibration file MUST be loaded first into the iDDS before the desired data files

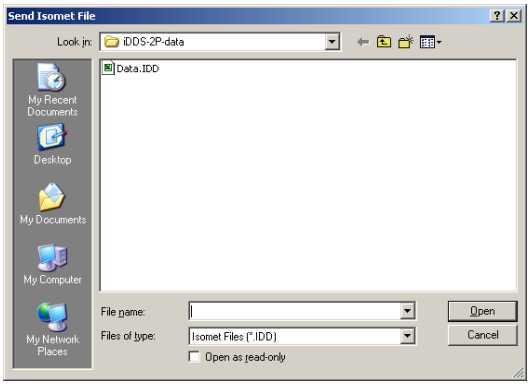
a: Load the Calibration file,
Select ***Send LUT*** in the ***Calibrate*** pull down menu from the Main Window.



Select the desired CAL file and ***OPEN***

During a successful download, the iDDS will respond and send 256 x **@c** character pairs. Completion is indicated with **@F** in the Serial I/O Data window.

b: Load the Data file
Select ***Send Isomet File*** in the ***File*** pull down menu.



Select the desired IDD file and ***OPEN***

During a successful download, the iDDS will respond and send a series of **@c** character pairs 4(one per Location). Completion is indicated with **@L** in the Serial I/O Data window. (@L may not be seen with USB download)

As a general rule, always load matched Calibration and Data tables.

Any valid Isomet Data file can be downloaded but will be modified by the currently installed Calibration table. If the Data file calls for a frequency that has not be entered during the calibration routine the iDDS will not generate a valid output.

A default calibration table is normally supplied for a given AO deflector type. This has entries for each frequency point across the device RF bandwidth.

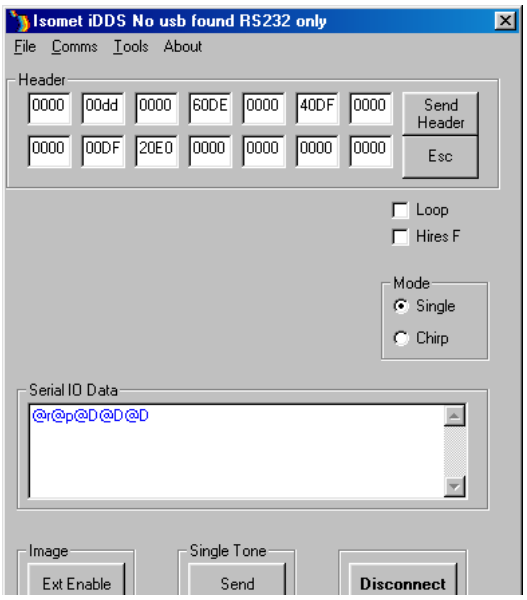
A spread sheet file is available to assist in the generation of the image data file.
Note: Setting of the control bits on the last entry is normally required

4.3 Loading Image Header

Certain control bytes are sent to the DDS once per trigger input via a Header written at the start of each Image data block within SRAM.

This data is input via the ***Header*** function in the ***Tools*** pull down menu

This Header data is typically programmed to reset the phase accumulators.
This ensures a known starting point prior to the output of the Image data.



The Header data is pre-programmed with the default values.
Under normal usage, the Header data will not require editing.

NOTE: A specific header must be loaded for Frequency Doubled Versions

4.4 Clock / Trigger Source

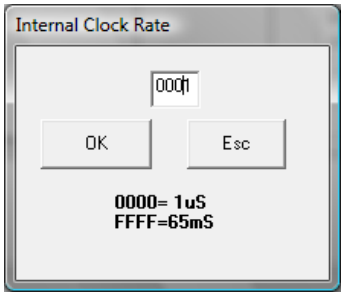
Trigger and clock signals are required to output the frequency pattern from the iDDS.
These can be internally generated or externally applied (connector J2)

The trigger input initiates the output sequence.
After this trigger, each applied clock edge will cause the iDDS output(s) to change according to image data stored in the *iDDS*.

Typically the last entry of the image data file includes an end-of-image (interrupt) bit.
With the ***LOOP*** radio button on the main menu is unchecked, the iDDS will stop, return to the start position and wait for the next trigger.

IF the ***LOOP*** radio button on the main menu is checked, the iDDS will continually loop around the data stored in the iDDS provided an active clock input is applied.

Internal
For the internal mode, an option is provided to adjust the data rate. The data output Clock can be internally generated and its rate is set via the ***Tools*** pull down menu and clicking on ***Int Clock Rate***



To enable the internal clock, click the ***Int Clk*** button on the MAIN menu.

The ***INT TRIG*** *(or 1 Shot)* button triggers the output sequence as described.

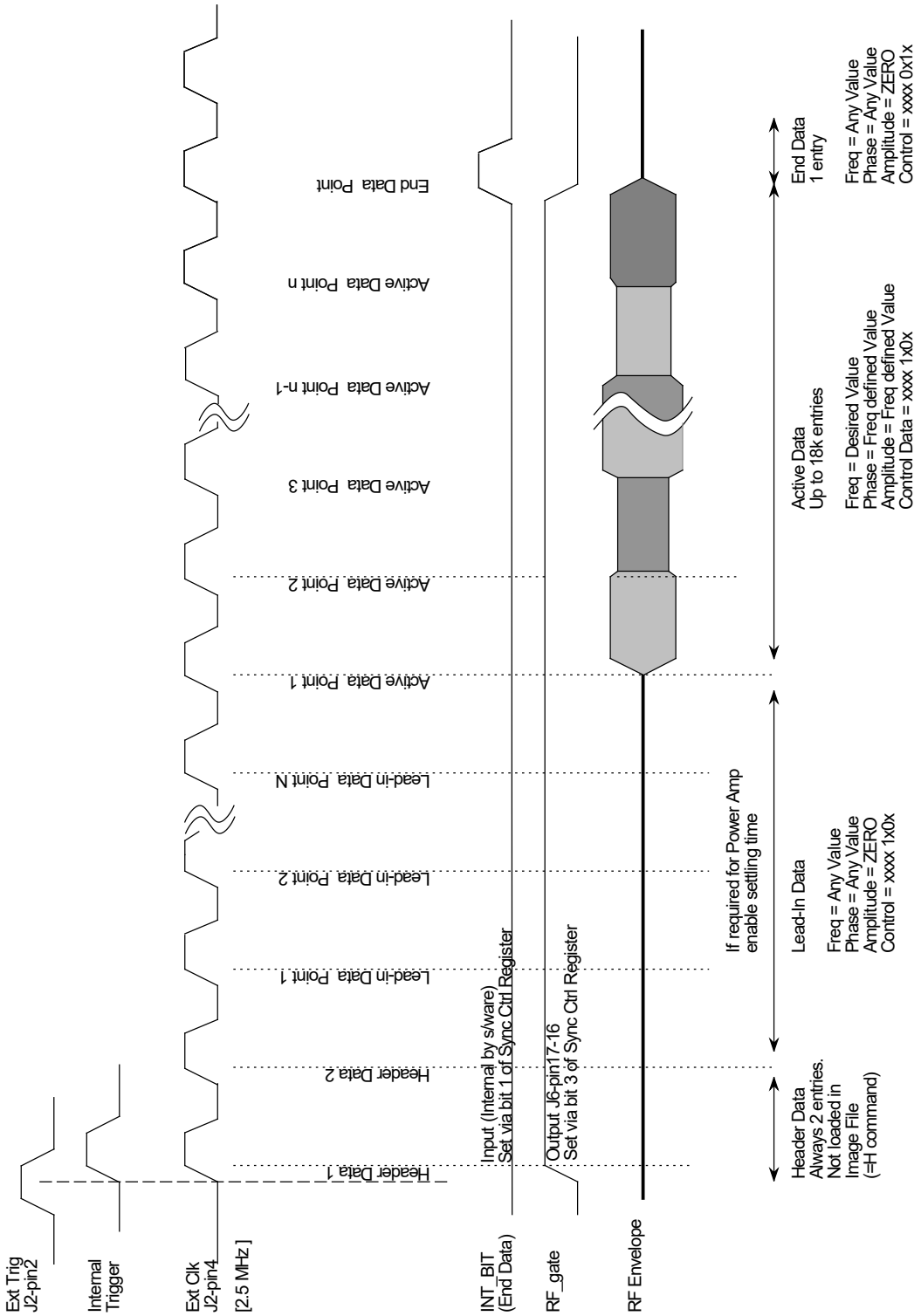
External

To enable the external inputs, click the ***Ext Enable*** button on the MAIN menu.
(This may also be labelled ***Init X*** or **Init Y**)

As above, the external trigger source will initiate the output sequence and the clock source will define the output data rate.

See Appendix A for connections

Typical Image mode timing diagram, External Control



5.0 Auxiliary Outputs

The iDDS features a selection of analog and digital I/O for general purpose use.

These are classified as static or dynamic.Static I/O are set and/or read on demand. Dynamic I/O are output synchronously with the frequency data in Image mode.

Please refer to the specific command descriptions with associated foot notes in Appendix D and the connector listings in Appendix E.

Static signals

Function	Channel / Ports	Connector	Command	Detail
Analog Output 12bit DAC, 0-10V	1	J4	=Y[n][n][n]	pg52
Analog Input, Unbuffered 16bit DAC, 0-6.25V	8	J6	=A[n]	pg48 & pg56
Analog Input, Buffered 16bit DAC, 0-2V	2	J4	=A[n]	pg48 & pg56
Analog Input, Buffered 16bit DAC, 0-10V	1	J4	=A[n]	pg48 & pg56
Analog Input, Buffered 16bit DAC, 0-10V	1	J4	=A[n]	pg48 & pg56
Bi-directional IO ports	8	J4	=m[n][n] : direction =o[n][n] : output set =I [n][n] : input read	Pg53 & pg56
RF_Gate Digital output	1	J6	=M[n]	pg50
Int_AMP Digital Input	1	J6	S/ware Output flag only (@eT)	pg55
Int_RF Digital Input	1	J6	S/ware Output flag only (@eK)	pg55

Dynamic signals

Programmed to change dynamically with Image and Data output modes.

Function	Channels / Ports	Connector	Description	Detail
Analog Output 12bit DAC	1	J3	Analog voltage representation of Frequency on Upper iDDS o/p	
Analog Output 12bit DAC	1	J3	Analog voltage representation of Amplitude on Lower iDDS o/p	
Logic levels Digital outputs	4	J2	Levels programmed in Image data (Synchronous Control Register bits 8,7,6,5)	pg38
RF_Gate Digital output	1	J6	Level programmed in Image data (Synchronous Control Register bit 4)	pg38

Special cases

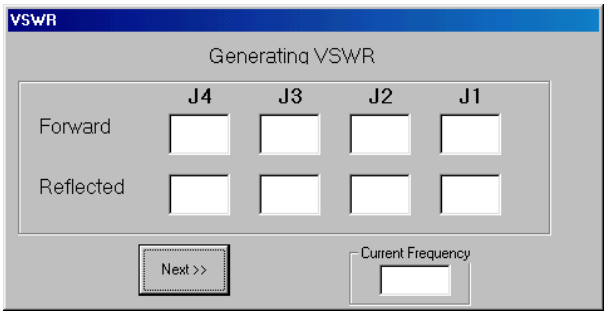
5.1 External Monitoring

When used with compatible amplifiers and AO devices, the iDDS can provide a control and monitoring signals

Example 1
VSWR monitoring of LS600-1011 AOD via the RFA1160/4 power amplifier

Using the Isomet GUI,

From the ***Tools*** pull down menu , select ***VSWR*** table



The iDDS will record the Forward and Reflected RF powers for each frequency, incremented by clicking on the ***Next*** button.When used with thee iDDS-2

Example 2
Temperature Interlock monitoring for LS600-1011 AOD via the RFA1160/4 power amplifier.

A change in level detected on either then INT_RF or INT_AMP inputs of J6 will generate a error message to the Host PC.

6.0 Programming

The iDDS is programmed and controlled from a Host PC via USB, RS485 or RS232 serial link.

Instructions are received and transmitted as ASCII Character strings. Characters 0-9, A-F, represent a Hex digit. i.e. 4 bits of data.

Each received instruction must be preceded with an "=" character.
The end of an instruction must be terminated with CR and LF
Receipt of 'Ctrl C' character will cancel the current instruction.

The first letter of the instruction is echoed back to the Host PC to acknowledge successful receipt and completion. Data transmitted back to the Host PC will be prefaced with "@" character.

It is advisable to wait for "@" acknowledge before sending the next instruction.

The DDS is capable of 48bit frequency resolution, 12bit amplitude resolution and 14bit phase (Phase only applies to dual output(-2) models).

The internal synthesiser ICs, utilize 8-bit data registers and a 6-bit address bus.
The register functions are listed below in **Appendix B**. Typically used registers highlighted in Blue.

7.0 Fixed Tone (single frequency output) from the iDDS-1 or -2

Data is programmed to a register using the =D command with the general format =D ddaa

Where: dd = data value
aa = register address

The register address can apply to one or both outputs of a dual iDDS-2
The same data values do not have to apply to both outputs

	Register Address (aa)		
	Upper O/P	Lower O/P	Both O/P
Data (dd)			
Freq MSB	84	44	C4
Freq	85	45	C5
Freq	86	46	C6
Freq LSB	87	47	C7
Amplitude MSB	A3	63	E3
Amplitude LSB	A4	64	E4
Phase MSB	80	40	C0
Phase LSB	81	41	C1

For a single output iDDS-1, use either the *Upper* or *Both* register addresses.

Table above shows addresses for 32bit Frequency resolution

7.1 Frequency Value

The frequency tuning word (FTW) is determined using the following equation:

$$FTW=(Desired\ Output\ Frequency \times 2^N)/SYSCLK$$

where: N = 48 maximum (16 typical)
Desired output frequency range = 10MHz < Freq <130 MHz
SYSCLK = 312.5 MHz

The FTW result must be rounded and converted to ASCII coded hex characters

Thus for 16 bit resolution, load the top 2 registers of Frequency_1 (e.g. C4, C5) with ASCII coded bytes. For 75.00 MHz, this equates to loading C4 with 3D and C5 with 70

7.2 Amplitude value

Amplitude is scaled to 12bits , (= 4095) maximum.

Amplitude = A%/100 x 4095

The result must be rounded and converted to ASCII coded hex characters.
Thus for full 12 bit resolution, load the 2 registers of Amplitude_1 (e.g. E3, E4) with ASCII coded bytes. For half maximum this equates to loading E3 with 08 and E4 with 00.

7.3 Phase value

Phase is scaled to 14bits , (= 16383) maximum.

Phase = Deg/360 x 16383

The result must be rounded and converted to ASCII coded hex characters.
Thus for full 14 bit resolution, load the 2 registers of Phase_1 (e.g. 40, 41 or 80, 81) with ASCII coded bytes. For 270 deg shift on lower output this equates to loading 40 with 2F and 41 with FF.

7.4 Initiating Output

a) Once all the desired registers are loaded, a single internal trigger (=I) and an update command (=U) must be issued. This clocks the new data into the DDS core.

b) The 'Asynchronous control register' (section 11) sets the operating mode of the iDDS. For single tone mode, this needs to be set at =E0C (or =E0F)

c) As a general rule proceed any instruction set with the clear command (=C) to ensure the iDDS is in the correct mode.

Thus the full command set for requesting an iDDS-2 to output 75MHz frequency at half maximum amplitude on both outputs with 270 deg phase shift on the lower is:

```
=C
=D3DC4
=D70C5
=D08E3
=D00E4
=D2F40
=DFF41
=I
=U
=E0C
```

8.0 Frequency Chirp (sweep output) from the iDDS-1 or -2

For this explanation, the frequency resolution is limited to 16 bits

The required registers for Chirp operation are listed in the table below.

	Register Address (aa)		
	Upper O/P	Lower O/P	Both O/P
Data (dd)			
Start Freq MSB	84	44	C4
Start Freq LSB	85	45	C5
Stop Freq MSB	AA	6A	CA
Stop Freq LSB	AB	6B	CB
Delta Freq MSB	90	50	D0
Delta Freq	91	51	D1
Delta Freq LSB	92	52	D2
Ramp rate MSB	9A	5A	DA
Ramp rate	9B	5B	DB
Ramp rate LSB	9C	5C	DC
Amplitude MSB	A3	63	E3
Amplitude LSB	A4	64	E4

8.1 Frequency Values

The Start, Stop and Delta frequency tuning words are calculated using the following equation:

$$FTW=(Desired\ Start\ (Stop,\ Delta)\ Frequency \times 2^N)/SYSCLK$$

where: N = 48 maximum (16 typical)
Desired output frequency range = 10MHz < Freq <130 MHz
SYSCLK = 312.5 MHz

$$\text{Delta Freq or freq resolution} = \frac{\text{Stop freq} - \text{Start freq}}{\text{Number of steps}}$$

The results must be rounded and converted to ASCII coded hex characters

8.2 Ramp Rate

The ramp rate defines the frequency sweep rate and is linked to the Delta Frequency value above. The smaller the rate multiplier (= greater Number of steps), the finer the frequency increment. Conversely, the fewer the Number of steps, the faster the min to max sweep rate.

$$\text{Ramp rate multiplier} = \left[\frac{\text{Total Chirp Time x 10\^6}}{\text{Number of steps x 3.2}} \right] - 1$$

where: Chirp time = milliseconds

The result must be rounded and converted to ASCII coded hex characters

Ramp rate multiplier MINIMUM value = 1

8.3 Amplitude value

Amplitude is scaled to 12bits , (= 4095) maximum.

Amplitude = A%/100 x 4095

The result must be rounded and converted to ASCII coded hex characters

8.4 Initiating Output

a) The IDDS must be placed into the correct mode for Chirp output
This is achieved via the =H command
Send '=H00000244DF' and '=H00000404DF'

b) The 'Asynchronous control register' (section11) sets the operating mode of the iDDS. For Chirp mode, this needs to be set to either =E20, if the sweep is to be triggered by via the host PC, or =EA0 if externally triggered (jnput on J2)

c) As a general rule proceed any instruction set with the clear command (=C) to ensure the iDDS is in the correct mode.

e.g. 75 -130MHz, 20usec sweep at half amplitude, both outputs active iDDS-2

=r	DDS reset
=C	Clear
=H00000244DF	Chirp config data
=H00000404DF	Chirp config data
=H0000030030	Set Synchronous control register (to 00 in this case) [3]
=D3DC4	Start Freq
=D70C5	Start Freq
=D6ACA	Stop Freq
=D7ECB	Stop Freq
=D00D0	Delta Freq
=D03D1	Delta Freq
=DB0D2	Delta Freq
=D00DA	Ramp rate
=D00DB	Ramp rate
=D01DC	Ramp rate
=D0863	Amplitude, Output RF2 [1]
=D0064	Amplitude, Output RF2 [1]
=D08A3	Amplitude, Output RF1 [1]
=D00A4	Amplitude, Output RF1 [1]
=D60E0	Sync Filter OFF
=U	Update clock

then for a s/w initiated "internal" trigger

=E20	Async Control register, Chirp mode Internal Trigger [2]
=I	Initiate the chirp output

or for an external trigger

=EA0	Async Control register, Chirp mode External Trigger [2]

and apply a 500nsec +ve TTL pulse to the TRIG input of connector J2 (No " =I" required)

Note:

1) In this case, Amplitude for the two outputs are programmed separately. The four could be combined into two entries i.e. =D08E3, =D00E4

2) =Exx is a logic control register (see section 11.1) and not a DDS Register. This sets the operating mode of the iDDS.

3) This line is optional in the Chirp control coding and included here for completeness. It defines the levels within the Synchronous Control register (See section 11.2)

It is possible to view the Chirp program code through the Isomet GUI Windows software when storing Chirp data into FLASH memory.

Direction of the frequency ramp output is defined by the logic level on pin 3 of J2

Low = Low to high frequency
High (or open circuit) = High to Low frequency

8.5 Storing Chirp Data in non-volatile Flash memory

Go to Chirp Menu (via <Chirp> Button in Mode box of main menu)
Enter start , stop freq, ramp time etc (section 3)

- Click on <Clear Flash> (iDDS will respond with @b)
- Click on <CLS> , to clear the Serial I/O Data window
- Check the <Save to DDS> box
- Click on <Chirp> button
  (Chirp data will be loaded to FLASH memory within the iDDS. The iDDS will respond with a series of "@a" character pairs)

- Place the iDDS in "Auto" mode by linking pins 12 and 24 of the 25way D type labeled "J2 SYNC-IO"
- Click on <CLS> , to clear the Serial I/O Data window
- Make a Hard Reset by momentarily linking pins 5 and 17 of the 25way D type labeled "J2 SYNC-IO" or cycling the DC power to the iDDS.

The iDDS will boot from the FLASH data previously loaded above. The Serial I/O Data window will display the code and iDDS responses for the Chirp data load.

Ignore non-ascii characters, the @ sign and the character(s) immediately following the @. These are the iDDS responses.

The actual Chirp code is given by the character's immediately following and including the" =" sign

9.0 iDDS Image Mode (Outputting sequential preloaded data)

9.1. Basic Concept

Pre-assigned data can loaded into the iDDS and clocked out at a rate defined by the user.

A frequency "image" is first downloaded to the iDDS. This image will contain frequency, amplitude and control data for each frequency point to be generated.

Once loaded, this image can be initiated using a single Start (Trigger) signal. The sequence of frequencies (as per the Image download) will be generated at a rate defined by an internal or externally provided clock signal. Once the complete image has been output, the iDDS output can be parked at a set frequency or a zero output and will await the next trigger input.

The minimum dwell time per frequency is about 1usec.
Typical applications include:

- High speed AO scanner optimization
- AOTF wavelength tuning
- Offset Frequency shift control between Bragg cell pairs.

9.2 Operation

As a frequency image is downloaded from the host PC into the iDDS, each frequency / amplitude data point is modified by the data stored in a calibration table.
This table contains phase data and amplitude scaling.

This is particularly useful in AO deflector applications where phase and /or amplitude weighting is applied to each frequency in order to equalise the output efficiency across a wide range of drive frequencies (= scan angles). A frequency specific phase offset is programmed between the iDDS-2 outputs. This is applied to the control launch angle of the acoustic wave within beam steered AO scanners. In this manner, the input Bragg angle is optimized regardless of the drive frequency of the AO device.

Phase data only applies to the dual output model iDDS-2.
For single output iDDS-1 models, the phase data is redundant. Nevertheless, the calibration table still needs to be loaded prior to the image file.

Typically the calibration amplitude / phase table for a single output iDDS-1 will be set for FFFFh/0000h for all 255 possible entries.

See sections 4 onwards in iDDS instruction manual for further explanation.

In total there are three steps to inputting an Image File:

Load: Look up table. (*.CAL file)
Load: Image file. (*. IDD file)
Load: Headers. (=Hnn command)

9.3 Image Data and Calibration file generation using Excel

Spreadsheets can be used to generate both the LUT and Image files.
The 'Analysis Tool pack' will need to be installed within Excel to enable Hex operations. (see ***Add-ins*** under ***Tools*** menu of Excel),

9.4 Look-up Table

A sample excel file is provided: **Phase LUT maker.xls** (or **Fx2 Phase LUT maker.xls** for frequency doubled versions).
This has two sheets, *Phase Calc* and *255-LUT*
The LUT file is always 255 entries long.
(Once loaded, it can be optimised from the Isomet GUI Windows operating software)

The user variables in Yellow highlighted areas will depend on the AO device. (Please request this data, if not supplied). Cells marked *(calc)* are calculated by Excel.
The LUT is defined by the Frequency tuning word (FTW) and not the absolute frequency itself. The LUT should be generated for a frequency range slightly larger that the device bandwidth.

Enter the lowest operating frequency in the 'Spot Freq Quick calc' to set the start FTW

The hex values in the final column R (in this example, cells R21:R108) **must be** copied and pasted *(Paste special>Values Only)* into column B of the *255-LUT* sheet, starting at the **LUT entry addr**. This start address is given in column Q of the *Phase Calc* sheet and found in column A of the *255-LUT* sheet by scrolling down.

Once pasted, copy B2:B257 into Windows "Note pad" and save with the extension .CAL.
This file MUST be exactly 255 entries x 8 hex characters.

Typical files are given e.g. ***MaxAMP_ZeroPHASE_allFREQ_LUT.cal***
(typical for iDDS-1)

532nm-FC102-P3-Amp700.cal
(typical for iDDS-2 used with the LS110 AOD)

As described above, the 14 bit Phase/16bit Amp scaling data pairs are 'fetched' on the fly from the LUT during the image load into SRAM, using the 9MSB's of the frequency value as a pointer to the FLASH memory location. A valid LUT must thus be installed prior to an Image load into memory

The LUT table is loaded using the Isomet GUI via the ***Tools*** pull down menu, ***Send LUT***. This file must have the extension ***.cal**

9.5 Image file

Once the *.cal file is loaded into non-volatile iDDS Flash memory, the Image data can be downloaded from the host PC.

For the standard iDDS models, a frequency 'image' of up to 18K points can be stored in 128K x 8bit Static RAM blocks within the iDDS. Images are loaded via the ***File*** pull down menu and must have the extension *.idd.

For extended memory versions, two frequency 'images' of up to 36K points each can be stored. In this case, a 'Bank_Switch', selects the start point for each of the two Images. This is software and hardware controllable (via connector J2).

Sample excel file is provided with a name similar to: **Image gen-IDD.xls** (or **Fx2 image gen-IDD.xls** for frequency doubled versions). This file will generate a 200 point image file.

The user variables in Yellow highlighted areas will depend on the AO device and desired operating range.

Enter the Start and Stop frequencies.
Enter Amplitude value. 0=off , 4095 = max. (This example sets the same value for all frequencies).
Enter any control bits required under the **Synchronous Control Register (includes Logic Outputs on J2)** section. NOTE: the Int_bit MUST ONLY be set to "1" on the final line. This marks the end-of-file

The final column R (in this example, cells R10:R212) will need to be copied into Windows "Note pad" and saved with the extension ***.idd** The first entry of this file gives the bank memory location (typically 0) and the number of image points (automatically counted by Excel).

The control data bits:

Mod4 Mod3 Mod2 Mod1 RF_gate Tacho Int_bit Laser_bit

are combined in The SYNC_CTRL byte, and can be left as default except bit_1 (Int_bit). This must be set to zero for all entries except the last point which is set to 1. This flags the end of the image data.

A typical file is given e.g. ***70-120M_AmpFAO-200stp.idd***

This is for a frequency ramp from 70Mhz to 120MHz in 0.25MHz steps (=200 points) in memory bank 0 . Amplitude 4000dec

9.6 Header Data

Image data is physically loaded in Image SRAM starting at address 15 (+ Bank offset)
i.e. 0000Fh and/or 8000Fh (Bank1)
SRAM address 00000h (80000h) is not utilised in 'RUN' mode due to address counter restrictions. SRAM address locations 00001h – 00014h (80001h-80014h) are available for header information.

To ensure robust operation, it is advisable to include the following instructions in the headers of each bank using '=H' command (or Header Option in Isomet Software):

The =H format is:
=H <Memory Bank> <SRAM Addr Location> <DDS Data><DDS Register Addr>

(Spaces added for clarity)

=H 0 00001 00 DD	DDS config
=H 0 00003 00 DF	DDS config
=H 0 00005 40 DF	Clear accumulator (at address less than 7)
=H 0 00008 00 DF	Toggle Clear accumulator (at address greater than 7)
=H 0 00009 60 E0 **	Disable Inverse Sinc Filter (Default)

** Alternative
=H 0 00009 20 E0 Enable Inverse Sinc Filter (If required)

An Update clock occurs at every 7th address count. The first two instructions zero the phase difference between two DDS outputs. These require an intermediate Update clock.

9.7 Frequency output

Once the Image is loaded, set (low) bits 3 and 2 of the Asynchronous Control Register (refer section 11). This switches the memory address bus from the internal uC to fast autonomous Address counters. The address counters increment according to the logic of the clock and trigger control signals, Ext_Clock & Ext_Trigger on connector J2 (or *Int Clk* from the Isomet GUI). Each clock edge will produce a new frequency profile at the iDDS output(s)

To enable the external signals (i.e TTL trigger on pin 2 of J2 and TTL clock on pin 4 of J2) set (high) bit 7 of the Asynchronous Control Register.
(or select ***Ext Enable*** button on the Isomet Software main menu).

Data will be output following the first trigger input at a rate defined by the clock input
Set (high) bit 6 of the Asynchronous Control Register if a continuous loop output is required.

For software controlled output, enable the internal cloak with command *=k* (or Select ***Int Clk)*** and trigger using command *=l* (or "press" on the ***Int Trig).***

The software clock rate is set via =K[n] command (or the ***Tools*** pull down menu and clicking on ***Int Clock Rate***).

If switching between internal and external clocking, be sure to set the Internal Clock rate to zero (=k0000) before selecting ***Ext Enable*** once more.

Be sure the correct memory Bank is selected as defined in the Image file. (pin 3 J2)

10 DataQ Mode (Outputting sequential preloaded data)

(If changing from Image to DataQ Modes or visa-versa apply a *Reset*)

Similar to the Image mode above except the full data set is written to the SRAMS without adaptation by the Calibration LUT data.

The Frequency Amplitude and Phase can be written to both, either or neither iDDS outputs depending on the upper 2 bits of the DDS register address

	Register Address (aa)		
	Upper O/P	Lower O/P	Both O/P
Data (dd)			
Freq MSB	84	44	C4
Freq	85	45	C5
Freq	86	46	C6
Freq	87	47	C7
Freq	88	48	C8
Freq LSB	89	49	C9
Amplitude MSB	A3	63	E3
Amplitude LSB	A4	64	E4
Phase MSB	80	40	C0
Phase LSB	81	41	C1
Sync Control	na	na	30

Table shows the register addresses for the full 48bit Frequency resolution

General form for each DDS register is: **ddaa**

d - Data nH <7:4> = upper 4 bits of DDS data
d - Data nL <3:0> = lower 4 bits of DDS data
a - Addr nH <7:4> = upper 4 bits of the DDS register address
a - Addr nL <3:0> = upper 4 bits of the DDS register address

The first two (dd) define the DDS register data value and are loaded into consecutive locations of the Image Data RAM (ID_SRAM), starting at location 15.

The second two (aa), define the respective DDS register address and are loaded into the associated, consecutive locations of the Image Address RAM (IR_SRAM), starting at location 15.

10.1 Operation

When in output mode, data is read out in 7-byte groups from the ID_SRAM and IR_SRAM memories into the DDS registers. Each cycle thus re-loads up to 7 registers. The iDDS outputs will reflect these new values at the end of each load cycle.
The 'load cycle-update output' sequence is repeated for every user applied External Clock or Int_Clock command.

The data in each group of 7 can be any mix of frequency, amplitude, phase and control data or can contain only one parameter (such as Frequency)

The DDS registers can be loaded in any order, or not all (if no change in value is required). However each "point" comprises of a fixed 7 user definable register values. If not all 7 registers are to be loaded, use Null values (00) in the unused entry.

In total there are two steps to inputting an DataQ File:

Load: Image file. (*. IRD file)
Load: Headers. (=Hnn command)

10.2 DataQ file

Sample excel file is provided with a name similar to: **DataQ gen-IRD.xls** .This will generate a 8 point Data file.

The user variables in Yellow highlighted areas will depend on the AO device and desired operating range.

Enter the desired Frequency and Amplitude and Phase for the Point.
Bank is "0" except larger memory versions of the iDDS.
Also select if the required values apply to the Upper , Lower or Both iDDS outputs
The Spreadsheet will apply the correct DDS register

Enter any control bits required under the **Synchronous Control Register (includes Logic Outputs on J2)** section. NOTE: the Int_bit MUST ONLY be set to "1" on the final line. This marks the end-of-file

The column F (in this example, cells G33:G40) will need to be copied into Windows "Note pad" and saved with the extension ***.ird** The first entry of this file gives the bank memory location (typically 0) and the number of image points (automatically counted by Excel).

The control data bits:

Mod4 Mod3 Mod2 Mod1 RF_gate Tacho Int_bit Laser_bit

are combined in The SYNC_CTRL byte, and can be left as default except bit_1 (Int_bit). This must be set to zero for all entries except the last point which is set to 1. This flags the end of the image data.

A typical file is given e.g. ***8-point.ird***

This generates a mix of frequencies, phases and amplitudes for a dual output iDDS-2.
The amplitude values for the final point are at zero in order to "see" the waveform terminate clearly on an oscilloscope.

10.3 Header Data

DataQ data is physically loaded in Image SRAM starting at address 15 (+ Bank offset) i.e. 0000Fh and/or 8000Fh (Bank1)
SRAM address 00000h (80000h) is not utilised in 'RUN' mode due to address counter restrictions. SRAM address locations 00001h – 00014h (80001h-80014h) are available for header information.

To ensure robust operation, it is advisable to include the following instructions in the headers of each bank using '=H' command (or Header Option in Isomet Software):

The =H format is:
=H <Memory Bank> <SRAM Addr Location> <DDS Data><DDS Register Addr>

(Spaces added for clarity)

=H 0 00001 40 DF	Clear accumulator (at address less than 7)
=H 0 00008 00 DF	Toggle Clear accumulator (at address greater than 7)
=H 0 00009 60 E0 **	Disable Inverse Sinc Filter (Default)

** Alternative
=H 0 00009 20 E0 Enable Inverse Sinc Filter (If required)

An Update clock occurs at every 7th address count. The first two instructions zero the phase difference between two DDS outputs. These require an intermediate Update clock.

10.4 Frequency output

Once the Image is loaded, set (low) bits 3 and 2 of the Asynchronous Control Register (refer section 11). This switches the memory address bus from the internal uC to fast autonomous Address counters. The address counters increment according to the logic of the clock and trigger control signals, Ext_Clock & Ext_Trigger on connector J2 (or *Int Clk* from the Isomet GUI). Each clock edge will produce a new frequency profile at the iDDS output(s)

To enable the external signals (i.e TTL trigger on pin 2 of J2 and TTL clock on pin 4 of J2) set (high) bit 7 of the Asynchronous Control Register.
(or select ***Ext Enable*** button on the Isomet Software main menu).

Data will be output following the first trigger input at a rate defined by the clock input
Set (high) bit 6 of the Asynchronous Control Register if a continuous loop output is required.

For software controlled output, enable the internal cloak with command *=k* (or Select ***Int Clk)*** and trigger using command *=l* (or "press" on the ***Int Trig).***

The software clock rate is set via =K[n] command (or the ***Tools*** pull down menu and clicking on ***Int Clock Rate***).

If switching between internal and external clocking, be sure to set the Internal Clock rate to zero (=k0000) before selecting ***Ext Enable*** once more.

Be sure the correct memory Bank is selected as defined in the Image file. (pin 3 J2)

11 Control Registers

The iDDS mode and control parameters are defined by two registers.

11.1 Asynchronous Control register ASCRL_REG

The Asynchronous Control register sets the fundamental operating mode of the iDDS
The value is programmed using the *=E[nn]* command.
He current setting of this register can be queried using the *=e* command

In Image or DataQ modes, this register also defines the source of the trigger and clock signals and whether the output cycles in a continuous loop fashion or singularly per trigger.

7	6	5	4	3	2	1	0 Bit
TC1 Int-Ext Trigger Source	TC2 Loop Single run or Cont'ous loop Out	Chirp Mode Select Active High. Chirp Mode Only	- 0	AD_CNTR Output Enable (-OEC) Active Low. Image, DataQ or Chirp Modes	ID_SRAM IR_SRAM Output Enable (-OES) Active Low. Image, DataQ or Chirp Modes	-RF Gate_Bit Force On Active Low. Overrides RF-gate Bit-3 of Sync Cntrl Reg	- 0

Bit 7 select table:

TC1	Trigger	Clock
0	Internal (uC)	Internal (uC)
1	External (J2)	External (J2)

Bit 6 select table:

TC2	Triggering of Image Data Output
0	Once to start, continuous loop around
1	Trigger required once per output sequence

Mode Select	Chirp Select		-RAM Select	
	Bit 5	*Bit4*	Bit3	Bit2
Direct (Single Tone) Mode	**0**	*0*	**1**	**1**
Memory load (Chirp, Image and DataQ)	**0**	*0*	**1**	**1**
Chirp Mode Output	**1**	*0*	**0**	**0**
Image Mode Output	**0**	*0*	**0**	**0**
DataQ Mode Output	**0**	*0*	**0**	**0**

Examples:

=E20 : Chirp Mode, Internal s/ware trigger, RF bit LOW
=E0F : Single Tone Mode, RF bit HIGH
=EC2 : Image Mode, External trigger, External Clock, RF bit HIGH

11.2 Synchronous Control register, SYNC CTRL_REG, (Address 30h)

The Synchronous Control register generates user programmable control signals. These are output synchronously with the Image data points. The most important bit is “INT_Bit”.

7	6	5	4	3	2	1	0 Bit
Mod-4	Mod-3	Mod-2	Mod-1	RF-Gate	TACHO	INT_Bit	(Unused)
On Connector/pin							
J2/9	J2/10	J2/6	J2/7	J6/17	(Internal)	(Internal)	-

Mod bits 1..4, and RF-Gate are Logic levels available on Connector J2/J6 and can be set ‘High’ or ‘Low’ as required to control external peripherals.

TACHO: Can be set ‘High’ and ‘Low’ on alternate entries to generate an alternating signal. This is can be used as a clock input to a counter within the micro-controller for diagnostic purposes. The value of the counter can be queried to determine the current output record position in the Image file. (see *=N* or *=n* command)

INT_Bit: Flags the End-of-Image (= last frequency point in a sequence).
This MUST be set to 1 on the last record entry ONLY.
It is applied internally to stop and/or reinitiate the iDDS output sequence.

The synchronous control register can be set directly with the =D command.
Its address is at 30h. e.g.

Command to clear Synchronous Control Register is ‘ =D0030’ (followed by =U, =I)

Typically the register is only programmed within the Image or DataQ files

Appendix A

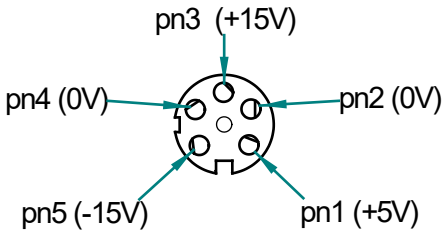
BASIC CONNECTIONS

- Connect DC voltages to J10

Voltage	Current	Conn	Pin
+12V (+15V max)	< 0.2A	J10	3
0V	RTN	J10	4
-12V (-15V max)	< 0.1A	J10	5
+5V (+5.2V max)	< 4.5A	J10	1
0V	RTN	J10	2

iDDS power cable socket

Internal view of **SOLDER** terminations



(= same view looking **into** bulkhead plug mounted in iDDS)

- Connect RF output(s) J7 and/or J8 to desired load.
  Pots set the maximum output level (0 – 2.5 mW).
  Default 1.0mW

- Depending on the iDDS model, connect the Host PC -

  USB to iDDS 'J1 Comms' via supplied USB cable

  or
  RS232 serial port to 'J1 Comms'
  Baud rate is fixed at 115Kbaud. No cross over required:

9way_D	PC Comms	iDDS J1
pin	2	2
pin	3	3
pin	5	5

  or
  RS485, 115Kbaud serial port to 'J1 Comms'

- Auxiliary functions are provided through connectors J3, J4 and J6.
  Not required for basic operation

- Main control signals are input through connector J2.

For “-D” versions the inputs and outputs are differential logic.
For all other versions only, the inputs are all single ended (TTL compatible).

If opto-isolated control signals have been specified, an additional isolated 5V supply input will be required on connector J2

+5V : J2/pn13
0V : J2/pn25

The standard iDDS configuration is non-isolated and the additional 5V supply will not be required on J2.

See table for detail

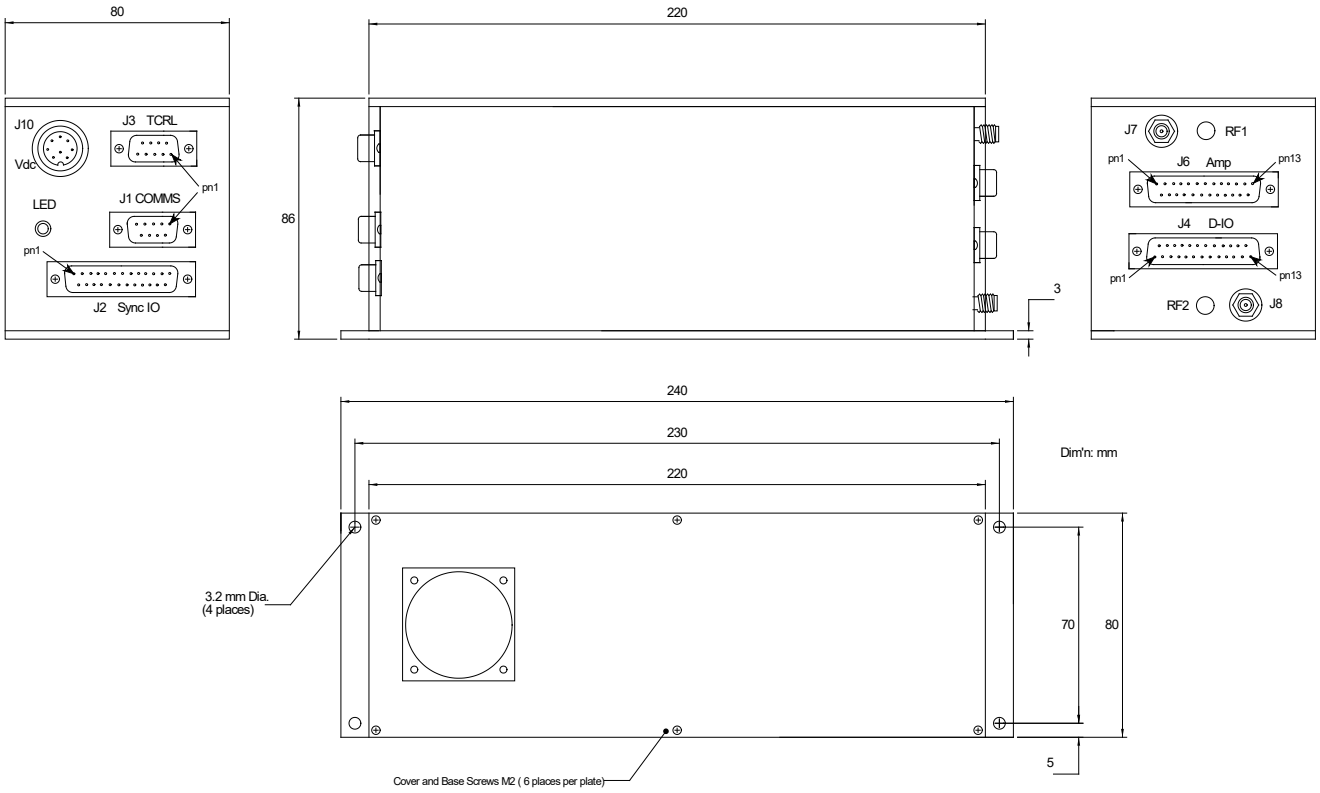
For –U and –SE variants all input signals on J2 have internal 1Kohm pull-ups.
No connection = Logic High

Control Signal (J2)

Signal	iDDS type -1 / -2 -1-A	iDDS type -SE -U	Single Tone	Image mode	Chirp Output
	Diff'l input	**TTL** input			
Trig	+Sig J2/2 - Sig J2/14	Sig J2/2 Gnd J2/14	Not Req'd	Start output sequence	Start Ramp
Clock	+Sig J2/4 - Sig J2/16	Sig J2/4 Gnd J2/16	Not Req'd	Output Data rate	Not required
Dir/Bank	+Sig J2/3 - Sig J2/15 -ve +ve	Sig J2/3 Gnd J2/15 Low (Closed) High (Open)	Not Req'd	Bank Select (larger memory versions only) SRAM Bank 0 SRAM Bank 1	Ramp Direction: Low to High High to Low
Reset	+Sig J2/5 - Sig J2/17 -ve +ve	Sig J2/5 Gnd J2/17 Low (Closed) High (Open)	Reset. (No output) Run		
	TTL input	**TTL** input			
Auto / PC	Sig J2/12 Gnd J2/24 High Low	Sig J2/12 Gnd J2/24 High (Open) Low (Closed)	Select iDDS control from Host PC or Auto boot (Auto_Bit / J2) Control via Host PC serial comms Boot from internal Flash (no PC req'd)		
Prog / Norm *	*Sig J2/11* *Gnd J2/23* *Low* *High*	*Sig J2/11* *Gnd J2/23* *Low (Closed)* *High (Open)*	*Load micro-controller core program. (BSL_Bit / J2)* *iDDS enters Boot strap mode allowing code download following a power cycle or RESET. Requires bespoke software such as FlashTW. Only required for Software updates.* *Normal Operating Mode.*		

* Prog/Norm signal is a "factory only" connection.

Outline Drawing



Dual output model *i*DDS-2 illustrated.
The output RF2/J8 does not apply to the single output models

Connector Functions given in Appendix C

Appendix B: DDS (AD9xxxx) Registers

Base Addr	iDDS Both o/p	-2 Lower only	-1 / -2 Upper only								Default Value
00	C0	40	80	Phase Adjust Register #1 <13:8> (Bits 15, 14 don't care)						**Phase_1**	00h
01	C1	41	81	Phase Adjust Register #1 <7:0>							
	00h										
02	-			Phase Adjust Register #2 <13:8:> (Bits 15, 14 don't care)						**Phase_2**	00h
03	-			Phase Adjust Register #2 <7:0>							
	00h										
04	C4	44	84	Frequency Tuning Word 1 <47:40>						**Frequency_1**	00h
05	C5	45	85	Frequency Tuning Word 1 <39:32>							00h
06	-			Frequency Tuning Word 1 <31:24>							00h
07	-			Frequency Tuning Word 1 <23:16>							00h
08	-			Frequency Tuning Word 1 <15:8>							00h
09	-			Frequency Tuning Word 1 <7:0>							00h
0A	CA	4A	8A	Frequency Tuning Word 2 <47:40>						**Frequency_2**	00h
0B	CB	4B	8B	Frequency Tuning Word 2 <39:32>							00h
0C	-			Frequency Tuning Word 2 <31:24>							00h
0D	-			Frequency Tuning Word 2 <23:16>							00h
0E	-			Frequency Tuning Word 2 <15:8>							00h
0F	-			Frequency Tuning Word 2 <7:0>							00h
10	D0	50	90	Delta Frequency Word <47:40>							
	00h										
11	D1	51	91	Delta Frequency Word <39:32>							
	00h										
12	D2	52	92	Delta Frequency Word <31:24>							
	00h										
13	D3	53	93	Delta Frequency Word <23:16>							
	00h										
14	-			Delta Frequency Word <15:8>							00h
15	-			Delta Frequency Word <7:0>							00h
16	-			Update Clock <31:24>							00h
17	-			Update Clock <23:16>							00h
18	-			Update Clock <15:8>							
	00h										
19	-			Update Clock <7:0>							40h
1A	DA	5A	9A	Ramp Rate Clock <19:16> (Bits 23, 22, 21, 20 don't care)							00h
1B	DB	5B	9B	Ramp Rate Clock <15:8>							00h
1C	DC	5C	9C	Ramp Rate Clock <7:0>							00h
				Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
1D	DD	5D	9D	Don't Care	Don't Care	Don't Care	Comp PD	Reserved Always L	QDAC PD	DAC P PD	DIG PD	10h
1E	DE	5E	9E	Don't Care	PLL Range	Bypass PLL	Ref Mult 4	Ref Mult 3	Ref Mult 2	Ref Mult 1	Ref Mult 0	64h
1F	DF	5F	9F	CLR ACC 1	CLR ACC 2	Triangle	SRC QDAC	Mode 2	Mode 1	Mode 0	**IN/-EX UD_Clk**	01h
20	E0	60	A0	Don't Care	**Bypass Inv Sinc**	OSK EN	OSK INT	Don't Care	Don't Care	LSB First	SDO Active	20h
21	E1	61	A1	Amplitude_2 <11:8> (Bits 15, 14, 13, 12 don't care)								00h
22	E2	62	A2	Amplitude_2 <7:0>				[Frequency Doubled Versions only]				00h
23	E3	63	A3	**Amplitude_1** <11:8> (Bits 15, 14, 13, 12 don't care)						[Output Shape Key Q Mult]		
	00h											
24	E4	64	A4	**Amplitude_1** <7:0>								00h

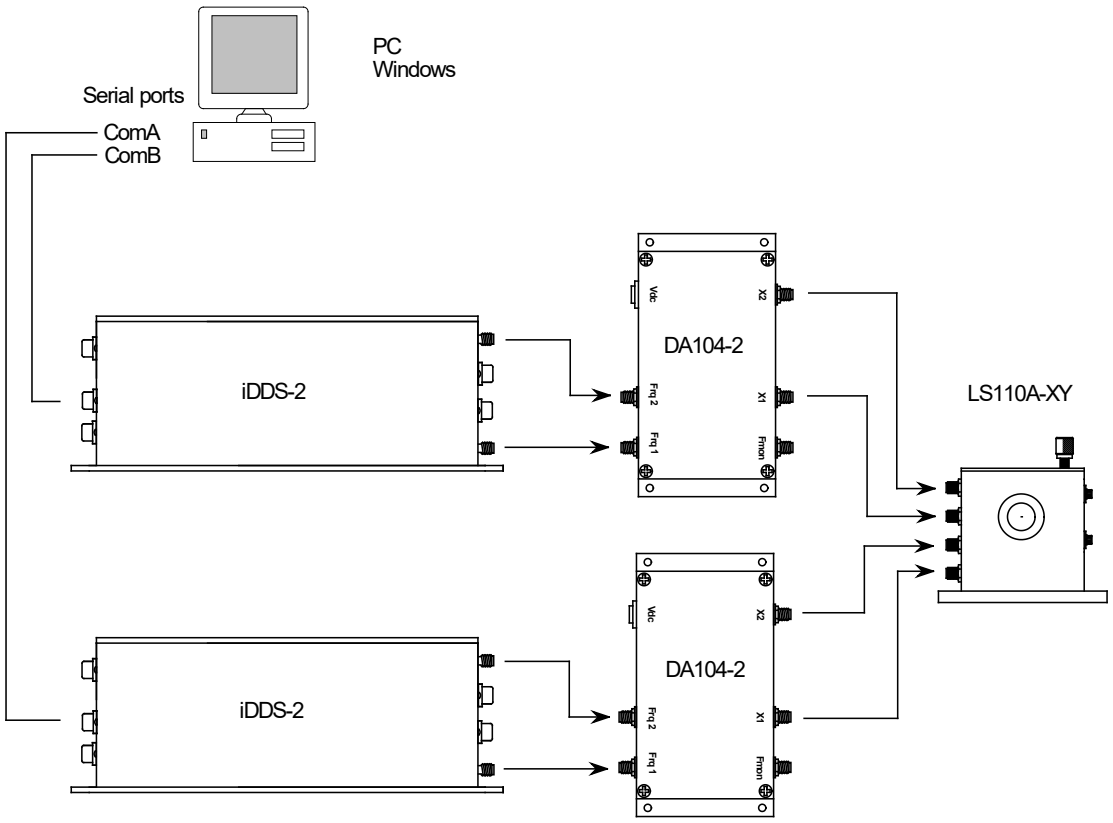
25	-	Output Shape Key Ramp Rate <7:0>	80h
26	-	QDAC <11:8> (Bits 15, 14, 13, 12 don't care)	00h
27	-	QDAC <7:0>	00h
		Data is required to be in two's complement format	

Non DDS register: Sync Control

-	**30**	**30**	**30**	**Mod4**	**Mod3**	**Mod2**	**Mod1**	**RFgate**	**Tacho**	**Int_Bit**	**(X)**	**00h**

Appendix C

Typical configuration with XY AO Deflector



iDDS-x Connector Summary

The signals described below apply to all operating modes of the iDDS-x unless stated.
All I/O logic levels are 5V TTL compatible.
Detailed information listed in connection tables Appendix E.

J1: USB or RS232 serial communication
Connect to PC

J2: Synchronous IO Signals: non-configurable
Inputs:

Trigger	(Image and Chirp Modes)
Clock Input	(Image Mode)
Chirp/Sweep direction	(Chirp mode)
Master Reset	
Power-On Command	
Boot strap	(Firmware upgrade only)

Outputs:
4off user programmable logic outputs

J3: Test IO Signals

Inputs:
FDATA : **DO NOT CONNECT**
SHAPE : **DO NOT CONNECT**

Outputs
DAC analog output proportional to frequency (Image Mode)
DAC analog output proportional to amplitude (Image Mode)

1 off user programmable logic output

J4: Static configurable logic IO (see pg 23)

Configurable IO:
8 off user programmable 5V logic I/O lines
3 off dedicated 5V logic lines

Outputs:
Static user programmable 0-10V analog output

J6: Monitor/control signals for compatible Power Amplifier modules or general use (see pg 23)

Inputs:
11 off user programmable ADC inputs
2 off dedicated switch contact inputs

Outputs:
1 off dedicated opto-isolated output

J7: RF_1 output

J8: RF_2 output.

Connections to J3, J4, and J6 are not necessary for basic operation

Appendix D

iDDS Instruction Set

Software Version(s): 59w3 to 77w3

D1.0 Host Communication

The *iDDS* communicates with a Host Controller via USB, RS232 or RS485 serial link.

Commands can be sent using a serial A communications program such as Hyperterminal

Instructions are received and transmitted as ASCII Character strings. A data value character 0-9, A-F, represent a Hex digit. i.e. 4 bits of data.

Each received instruction must be preceded with an "=" character.
The end of an instruction must be terminated with CR and LF
Receipt of 'Ctrl C' character will cancel the current instruction.

The first letter of the instruction is echoed back to the Host PC to acknowledge successful receipt and completion. Data transmitted back to the Host PC will be prefaced with "@" character.

An error character will be echoed back to the Host if the data format is not recognised. E.g. expected 4 bytes following the instruction character but only received 3. (see Transmitted Instruction Set)

For Image and LUT data file downloads, 16-bit CRC error control is adopted. CRC check sum can be made at each Image record point, on a block of data or the complete Image. Positive acknowledge (@c) will be issued by the *iDDS* after each record (point) is received correctly, otherwise the Error character (@K) will be transmitted. The Host should wait for the acknowledge character before transmitting the next record / point.

Certain Instructions are not permitted during an output sequence from Image SRAM (LUT mode).

A single '@R' followed by 'OI' is sent on Power-on to confirm integrity of the communication link.

To avoid contentions, operating mode changes should be proceeded with =C (clear) command.

D1.1 Received Instruction Set: Upper case

Instruction	Description	[Character] following Instruction		Restriction	Note
=A [1]	Request ADC conversion	[1]	If [1] = hex digit (0-F), Fixed channel conversion on the channel number specified. If [1] = 'V', Scan channel conversion on Ch 0 > 7 (e.g. all VSWR outputs from RFA1160-4)	See @A	5
=B [1]	-Force LASER_ Bit	[1]	If [1] = 'H', Set HIGH = Laser OFF If [1] = 'L', Set LOW = Laser ON		
=C	CLEAR		Clear Counters, Latches and Buffers WITHOUT resetting uC or changing state of RF-gate or LASER_Bit. Set –CS for DIRECT Mode Reset DDS1/DDS2 Set to Single Tone Mode, no Inv Sinc filters Mask external Trig/Clock (i.e. ASCRL_REG= 0000 11xx)		
=D [1][2][3][4]	Direct Mode Will place iDDS in direct mode and load data to specified address (LUT multiplication not applied)	[1] [2] [3] [4]	Data <7:4> Data <3:0> Address <7:4> Address <3:0>	Not allowed during IMAGE Mode. (Typically followed by =U)	3
=E [1][2]	Set ASCRL_Reg	[1] [2]	Bits <7:4> Bits <3:0> See Appendix B	Default '0Fh'	

=F[1]<>[6] …[7]<>[20] [x 256 points]	FLASH Download	 [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [#]	Load Merged Phase/Amplitude LUT All 256 locations must be loaded Top 9 bits of frequency tuning DWord (FTW) points to LUT address in Flash sector. # Image Points <15:12> = 0 # Image Points <11:8> = 1 # Image Points <7:4> = 0 # Image Points <3:0> = 0 <CR> <LF> Amp Data <15:12> (0) Amp Data <11:8> Amp Data <7:4> Amp Data <3:0> Phase Data <13:12> Phase Data <11:8> Phase Data <7:4> Phase Data <3:0> CRC<15:12> CRC<11:8> CRC<7:4> CRC<3:0> <CR> <LF> Steps [7]:[20] repeated 256 x (Program download initiated at Power-On depending on BSL Link on J2)	Not allowed during IMAGE Mode See ‘f’	
=G	GO in IMAGE mode		Zero TACHO counter register Enable Output Sequence (IMAGE Mode). RF-gate and LASER_Bit defined by Image data Allow external Trig/Clock (ASCRL_REG = C3h)	Precede with CLEAR command	
=H [1][2][3][4] …[5][6][7][8] …[9][10]	Load both ID_SRAM and IR_SRAM at specified address (Debug)	[1] [2] [3] [4] [5] [6] [7] [8] [9] [10]	Bank Select (Boundary at 80000h) SRAM Address <19:17> SRAM Address <16:13> SRAM Address <12:9> SRAM Address <8:5> SRAM Address <4:1> ID_SRAM Data <7:4> ID_SRAM Data <3:0> IR_SRAM Data <7:4> (=DDS register addr) IR_SRAM Data <3:0> (=DDS register addr)	Not allowed during In-direct Mode	2
=I	Internal Trigger		Force trigger signal (single shot)	Effective according to (TC1/TC2 of ASCRL_REG)	
=J [1]	Set Clock/Trig Source Re : ACSRL_REG		If [1] = ‘E’, Set TC1=TC2=HIGH If [1] = ‘I’, Set TC1=TC2=LOW If [1] = ‘T’, Set TC1=HIGH, TC2=LOW If [1] = ‘C’, Set TC1=LOW, TC2=HIGH	Special case of ‘E’	
=K [1][2][3][4]	Internal Run Clock rate (Min’ freq = KFFFF)	[1] [2] [3] [4]	Period Counter Data <15:12> Period Counter Data <11:8> Period Counter Data <7:4> Period Counter Data <3:0>	See ‘k’	9

=L[1]<>[11] ….[12]<>[26] [# Points]	Download “Image” File	[1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [#]	Bank Select # Image Points <15:12> # Image Points <11:8> # Image Points <7:4> # Image Points <3:0> CRC<15:12> CRC<11:8> CRC<7:4> CRC<3:0> <CR> <LF> Freq Data <15:12> Freq Data <11:8> Freq Data <7:4> Freq Data <3:0> Amplitude Data <11:8> Amplitude Data <7:4> Amplitude Data <3:0> Sync Control Data <7:4> Sync Control Data <3:0> CRC<15:12> CRC<11:8> CRC<7:4> CRC<3:0> <CR> <LF> Sequence [12]…[26] repeat for # Points	Not allowed during IMAGE Mode.	3,7,8
=M [1]	-Force RF_ gate	[1]	If [1] = ‘H’, Set HIGH = RF off If [1] = ‘L’, Set LOW = RF on		
=N	*Tacho Counter Value*		*Read Output position in Image*	*Reset after each Interrupt_bit or at each =G*	*12*
=P	-				

=Q[1]<>[11] ….[12]<>[45] [# Points]	Download “DataQ” file	[1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [#]	Bank Select # Image Points <15:12> # Image Points <11:8> # Image Points <7:4> # Image Points <3:0> CRC<15:12> CRC<11:8> CRC<7:4> CRC<3:0> <CR> <LF> Data AH <7:4> Data AL <3:0> Addr AH <7:4> Addr AL <3:0> Data BH <7:4> Data BL <3:0> Addr BH <7:4> Addr BL <3:0> Data CH <7:4> Data CL <3:0> Addr CH <7:4> Addr CL <3:0> Data DH <7:4> Data DL <3:0> Addr DH <7:4> Addr DL <3:0> Data EH <7:4> Data EL <3:0> Addr EH <7:4> Addr EL <3:0> Data FH <7:4> Data FL <3:0> Addr FH <7:4> Addr FL <3:0> Data GH <7:4> Data GL <3:0> Addr GH <7:4> Addr GL <3:0> CRC<15:12> CRC<11:8> CRC<7:4> CRC<3:0> <CR> <LF> Sequence [12]…[45] repeat for # Points	Not allowed during RUN Mode.	15

=R	RESET		Clear SYCRL_REG (LASER_BIT, RF_gate Off). Mask external Trig/Clock (ASCRL_REG = 0Fh) Reset uC, Clear SRAM Clear Tacho / Trigger Counter		
=S	STOP		Stop at end of sequence (INTERRUPT_bit) Clear SYCRL_REG (LASER_BIT, RF_gate Off). Mask external Trig/Clock (TC1=TC2=0 ASCRL_REG)	Restarts on '=G'	
=T	Terminate		Terminate sequence without completing. Clear SYCRL_REG (LASER_BIT, RF_gate Off). Mask external Trig/Clock (TC1=TC2=0 ASCRL_REG)	Restarts on '=G'	
=U	Update Clock		Send SINGLE Update clock pulse (Direct Mode) i.e. One period of '=Kxxxx' clock setting	Valid in Direct Mode only	
=V	Verify		Read Back last command sent		
=W[1]	Write back Image Data	[1]	Debug op. Write Image data to Host Must precede by setting ASCRL_REG bit_3 High and bit_2 Low e.g. ASCRL_REG =E0B (laser and RF OFF) ASCRL_REG =E0A (laser ON / RF OFF) If [1] = '0', Bank (0) If [1] = '1', Bank (1)	Not allowed during IMAGE Mode. SRAM outputs must be enabled	
=Y[1][2][3]	Load 12-bit Async DAC	[1] [2] [3]	Data <11:8> Data <7:4> Data <3:0>	Not allowed during IMAGE Mode	4
=Z	Zero SRAM		Clear ID_SRAM and IR_SRAM to zero	Not allowed during IMAGE Mode	See 'z'

D1.2 Received Instruction Set: Lower case

Instruction	Description	[Character] following Instruction		Restriction	Note
=a[1]	Store to Boot Flash Sector.		Append next instruction [1] to Boot Flash Sector		11
=b	Clear Boot Flash Sector				
=c	Clear Trigger Counter				
=d[1][2]	Read DDS register	[1] [2]	Bits 7>4, Reg Addr Bits 3>0, Reg Addr Debug feature Precede with =E0C or =E0F	Not allowed during IMAGE or CHIRP Mode See @ d [1][2]	14
=e	Read ASCRL_Reg			See @ e [1][2]	
=f	Read LUT		Read all 255 locations of LUT sector. Comma delimited FTW(9MSB), Amplitude, Phase		
=i	Programmable logic port, Read levels		Read Input and Output levels	See @ i [1][2][3][4]	
=k	Run Internal Update Clock		Clock rate set be 'K' command above. Required after first =Kxxxx command.	Set 'K' value first. Effective according to (TC1/TC2 of ASCRL_REG	
=l [1]	Load FLASH – Test Option	[1]	If [1] = 'd', Set Amplitude FFFh and Phase 0000h all locations If [1] = 't', Set Amplitude FFFh and top 8 bits of Phase to LUT address index number		
=m[1][2]	Programmable logic port, Bit selectable direction	[1] [2]	Bits 7>4, 1=o/p, 0=i/p Bits 3>0, 1=o/p, 0=i/p		6
=o[1][2]	Programmable logic port, Set Bit output levels	[1] [2]	Bits 7>4, Bits 3>0,	Valid for output assigned pins See =m[1][2]	
=n	Trigger Counter Value		Read number of (Input triggers)/2	Clears after RESET or =c	13
=p	Preset DDS		Clear both accumulators Disable Inverse Sinc Filter	Not effective during IMAGE Mode	

=r	Reset		Send Reset to DDS and Hardware Only Resets SRAM address counters to zero uC not Reset	Output continues following '=r' starting at Image point 0	
=v	Read Software Version			See @ v [1][2][3][4]	
=z[1][2]	Fill SRAM with fixed data – Test Option	[1] [2]	Data <7:4> Data <3:0>	Not allowed during IMAGE Mode	4

D1.3 Transmitted Instruction Set

Instruction	Description	[Character] following Instruction		Note
@a	Acknowledge Boot Flash Sector load			
@A [1][2][3][4][5]	Send 10bit ADC conversion result(s)	[1] [2] [3] [4] [5]	Number of channel conversions to follow. Channel # ADC Data <9:8> ADC Data <7:4> ADC Data <3:0> Sequence [2]…[5] repeat for [1]	See =A
@c	CRC Acknowledge		Record OK	
@d [1][2]	DDS IC register contents	[1] [2]	Bits 7>4, Bits 3>0	14
@e [1] (or)	Error	[1]	If [1] = 'T', Over temp AOD If [1] = 'K', Over temp Amp If [1] = 'D', Optical detector warning If [1] = 'C', Comms error If [1] = 'I', Instruction error, unrecognised character If [1] = 'X', Instruction error, unexpected character If [1] = 'M', Instruction error, Not allowed in current operating mode	
@e [1][2]	Async Control Register Contents	[1] [2]	Bits 7>4, Bits 3>0	See A4.0
@ i [1][2][3][4]	Programmable logic port, Read Bit output levels	[1] [2] [3] [4]	Bits 15>12, read only Bits 11>8, read only Bits 7>4, IO selectable (see =m..) Bits 3>0, IO selectable (see =m..)	See =i
@K	CRC Error		Re-transmit	
@N [1]<>][8]	Trigger Counter Value (Triggers received / 2)	[1] [2] [3] [4] [5] [6] [7] [8]	Counter Data <28:31> Counter Data <24:27> Counter Data <20:23> Counter Data <16:19> Counter Data <15:12> Counter Data <11:8> Counter Data <7:4> Counter Data <3:0>	See =N
@O[1]	Optical Detection Valid			
@R	Return R		Confirms communication following Reset or Power-On	

@v[1][2][3][4]		[1] [2] [3] [4]	Software version Major revision Minor revision W = windows (CR+LF) , L= Linux (CR only) version Baudrate; 1=9600, 2=57k6, 3=115K, 0=other	See =v
@V [1]	Status	[1]	Last Command Instruction Character	
@W [1][2][3][4]… ….[5][6][7][8].. …[# Points]	Read back Image	[1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]	Freq Data <15:12> Freq Data <11:8> Freq Data <7:4> Freq Data <3:0> Amplitude Data <11:8> Amplitude Data <7:4> Amplitude Data <3:0> Phase Data <13:12> Phase Data <11:8> Phase Data <7:4> Phase Data <3:0> Sync Control Data <7:4> Sync Control Data <3:0> Sequence [1]…[13] repeats	See=W[x]

Notes:

1: uC Chip select –CS0 active

2: uC Chip select –CS2 active

3: uC Chip select –CS3 active

4: uC Chip select –CS4 active

5: Full scale 10bit ADC (1024)

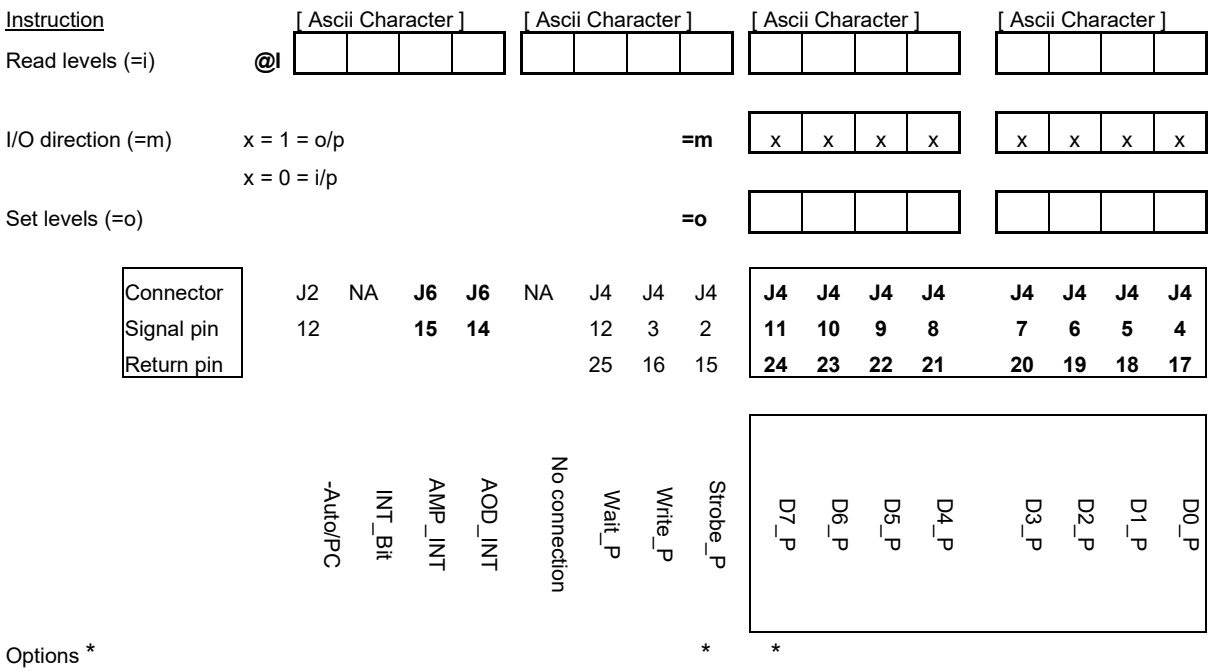
Channels 0 > 7	0- 6.25V :	Forward and Reflected RF power *
Channels 8	0-2.0V :	AOD temperature 10mV/°C (= 5.12 binary/°C)*
Channels 9	0-2.0V :	AMP temperature 10mV/°C (= 5.12 binary/°C)*
Channels 10,11	0-10V :	Buffered inputs
Channels 12	N/A :	Optional unbuffered input
Channels 13,14,15	Not used	

* Typical dedicated application when used with RFA1160/4

Cont'd

6: Bit programmable port signals:
Bits D0_P > D7_P available on Connector J4
Bit D7_P normally connected. Option to remove for compatibility with earlier h/ware versions

Signal-Connection Map



7: Image data from a host PC is loaded into the Image SRAM starting at address 15+ Bank offset i.e. 0000Fh and for large memory versions 8000Fh (Bank1)

Amplitude data is normalized by the 12bit Amplitude look up table (ALUT) value.
Phase data is determined by the Frequency data value using a Phase look up table (PLUT)
Control data is unmodified.

The result is a series of 7 data words per image point

Frequency:	2 words
Amplitude:	2 words
Phase:	2 word
Synchronous Control data:	1 word

Cont'd

8: Image data is physically loaded in Image SRAM starting at address 15 (+ Bank offset)
i.e. 0000Fh and/or 8000Fh (Bank1)
SRAM address 00000h (80000h) is not utilised in 'RUN' mode due to address counter restrictions.
SRAM address locations 00001h – 00014h (80001h-80014h) are available for header information.

To ensure robust operation, it is advisable to include the following instructions in the headers of each bank using '=H' command (or Header Option in Isomet Software):

(Spaces added for clarity)

=H 0 00001 40 DF	Clear accumulator (at address less than 7)
=H 0 00008 00 DF	Toggle Clear accumulator (at address greater than 7)
=H 0 00009 60 E0	Disable Inverse Sinc Filter

An Update clock occurs at every 7th address count.
The first two instructions zero the phase difference between two DDS outputs and require an intermediate Update clock .

9: Minimum rate = KFFFF or Period ≈ 65msec
Maximum rate = K0000 or Period ≈ 1usec

10: Phase detector not used in current build.

11: Auto Boot mode. iDDS operates at power on, (no PC commands required) using a command sequence previously loaded into a sector of Flash.

The =b command erases the flash sector that is to be used for this 'auto mode' initialisation.

The =a command is used to prepend any standard command. This will cause the command to be routed and stored in the flash sector at the end of the current list of stored commands

12: Optional alternative application for the Internal counter. (Not user selectable)
If applied, =n command not valid (see note 13)

13: The trigger counter increments for every 2 input triggers.
In reading the trigger counter during active Chirp/Image output operation, some counts may be missed.

14: Read DDS registers
For dual output models, internal logic prevents simultaneous read of both DDS chips. Appendix B shows the register function and addresses.

The iDDS unit needs to be in a static mode to read the register contents.
Thus following a Chirp data load or during the Chirp operation, first halt the iDDS by entering =E0C or =E0F.
(Once the reads are complete, the Chirp operation can be reinstated by entering =EA0 or =EA3)

Query the register of interest with the command =dnn
The iDDS will respond with @dmm

A response of @dD0 normally indicates missing or invalid register

e.g Model iDDS-1 variant, programmed for a 75-125MHz chirp with 16KHz frequency increment, fastest Ramp rate clock and at half maximum amplitude:

Parameter	Enter	Response
Start Frequency (MSW)	=d84	@d3D
Start Frequency	=d85	@d70
Stop Frequency (MSW)	=d8A	@d66
Stop Frequency	=d8B	@d66
Delta Frequency (MSW)	=d90	@d00
Delta Frequency	=d91	@d03
Delta Frequency	=d92	@d5A
Ramp Rate Clock (MSW)	=d9A	@d00
Ramp Rate Clock	=d9B	@d00
Ramp Rate Clock	=d9C	@d01
Amplitude 1 (MSW)	=dA3	@d08
Amplitude 1	=dA4	@d00

15: DataQ Mode (=Q command)

Each “point” comprises of 7 potential DDS register bytes A,B,C,D,E,F,G and are loaded as pairs of ascii coded characters.

General form for each DDS register is: **ddaa**

d - Data nH <7:4> = upper 4 bits of DDS data
d - Data nL <3:0> = lower 4 bits of DDS data
a - Addr nH <7:4> = upper 4 bits of the DDS register address
a - Addr nL <3:0> = upper 4 bits of the DDS register address

Where n = A,B,C,D,E,F,G

The first two define the DDS register data value and are loaded into consecutive locations of the Image Data SRAM (ID_SRAM), starting at location 15.

The second two, define the respective DDS register address and are loaded into the associated, consecutive locations of the Image Address SRAM (IR_SRAM), starting at location 15.

Potential register addresses are listed on pg44

Appendix E

Connector Tables

Signal Designation	Signal	Type	Description	Connector	Label	Pin
RF_1	Output	0- >2mW 50 ohm	RF output at specified freq.	SMA	J7	
RF_2	*Output (-2)*	*0- >2mW 50 ohm*	*Phase modified RF output at specified freq.*	*SMA*	*J8*	
A11_IN (IR_Det_IN)	Input	Analog	10bit ADC input (0-10V buffered)	25D-type Skt	J4	1
A11_rtn					J4	14
A12_IN (standard) or *Strobe_P (option P)*	Input	Analog *TTL Logic*	10bit ADC input (0-10V) *Parallel Data strobe*	25D-type Skt	J4	2
A12_rtn or *Strobe_rtn (opt'n P)*					J4	15
Write_P	I/O	TTL Logic	Digital I/O	25D-type Skt	J4	3
Rtn						16
D0_P	I/O	TTL Logic	Digital I/O D0	25D-type Skt	J4	4
D0_P_rtn					J4	17
D1_P	I/O	TTL Logic	Digital I/O D1	25D-type Skt	J4	5
D1_P_rtn					J4	18
D2_P	I/O	TTL Logic	Digital I/O D2	25D-type Skt	J4	6
D2_P_rtn					J4	19
D3_P	I/O	TTL Logic	Digital I/O D3	25D-type Skt	J4	7
D3_P_rtn					J4	20
D4_P	I/O	TTL Logic	Digital I/O D4	25D-type Skt	J4	8
D4_P_rtn					J4	21
D5_P	I/O	TTL Logic	Digital I/O D5	25D-type Skt	J4	9
D5_P_rtn					J4	22
D6_P	I/O	TTL Logic	Digital I/O D6	25D-type Skt	J4	10
D6_P_rtn					J4	23
D7_Bit	I/O	TTL Logic	Digital I/O D7	25D-type Skt	J4	11
D7_P_rtn					J4	24
Wait	I/O	TTL Logic	Digital I/O	25D-type Skt	J4	12
rtn					J4	25
BIAS_Out	Output	Analog	0-10V DAC Output Voltage	25D-type Skt	J4	13
BIAS_rtn	Output			25D-type Skt	J4	25

Signal Designation	Signal	Type	Description	Connector	Label	Pin
A0_IN (FWD_1)	Input	Analog	10bit ADC input (0- 6.25V)	25D-type Plg	J6	1
A1_IN (REV_1)	Input	Analog	10bit ADC input (0- 6.25V)	25D-type Plg	J6	2
Rtn_1			Signal return	25D-type Plg	J6	18
A2_IN (FWD_2)	Input	Analog	10bit ADC input (0- 6.25V)	25D-type Plg	J6	3
A3_IN (REV_2)	Input	Analog	10bit ADC input (0- 6.25V)	25D-type Plg	J6	4
Rtn_2			Signal return	25D-type Plg	J6	19
A4_IN (FWD_3)	Input	Analog	10bit ADC input (0- 6.25V)	25D-type Plg	J6	5
A5_IN (REV_3)	Input	Analog	10bit ADC input (0- 6.25V)	25D-type Plg	J6	6
Rtn_3			Signal return	25D-type Plg	J6	20
A6_IN (FWD_4)	Input	Analog	10bit ADC input (0- 6.25V)	25D-type Plg	J6	7
A7_IN (REV_4)	Input	Analog	10bit ADC input (0- 6.25V)	25D-type Plg	J6	8
Rtn_4			Signal return	25D-type Plg	J6	21
A8_IN (T_Amp)	Input	Analog	10bit ADC input (0- 2.0V)	25D-type Plg	J6	10
A8_rtn			Signal return	25D-type Plg	J6	22
A9_IN (T_AOD)	Input	Analog	10bit ADC input (0- 2.0V)	25D-type Plg	J6	9
A9_rtn			Signal return	25D-type Plg	J6	23
RF_gate	Output	Logic	* RF enable (Opto)	25D-type Plg	J6	17
RF_gate_rtn				25D-type Plg	J6	16
INT-Amp	Input	Logic	* Amp' Thermal interlock Status	25D-type Plg	J6	15
INT-rtn	Input		* Signal return	25D-type Plg	J6	25
INT-AOD	Input	Logic	* AOD Thermal interlock Status	25D-type Plg	J6	14
A10_IN	Input	Analog	10bit ADC input (0- 10V, buffered)	25D-type Plg	J6	11
A10_rtn			Signal return	25D-type Plg	J6	24
Nc				25D-type Plg	J6	12
Nc				25D-type Plg	J6	13

( ) / * : where Amplifier and /or AO device fitted with appropriate sensors

Signal Designation	Signal	Type	Description	Connector	Label	Pin
RS232	Rtn		Via internal 100ohms	9D-type Skt	J1	5
RS232	In		Serial comm. to Host	9D-type Skt	J1	3
RS232	Out		Serial comm. to Host	9D-type Skt	J1	2
USB			USB-rst	*9D-type Skt*	*J1*	*6*
USB			USB-dm	*9D-type Skt*	*J1*	*7*
USB			USB-dp	*9D-type Skt*	*J1*	*8*
USB			Gnd	*9D-type Skt*	*J1*	*9*
- OR -						
RS485	*In+*	*Diff Logic*	*Serial comm. to Host*	*9D-type Skt*	*J1*	*8*
RS485	*In-*		*Serial comm. to Host*	*9D-type Skt*	*J1*	*3*
RS485	*Out+*	*Diff Logic*	*Serial comm. to Host*	*9D-type Skt*	*J1*	*7*
RS485	*Out-*		*Serial comm. to Host*	*9D-type Skt*	*J1*	*2*
RS485	*Rtn*			*9D-type Skt*	*J1*	*4*
RS485	*Rtn*			*9D-type Skt*	*J1*	*6*
Gnd			*Via internal 100ohms*	*9D-type Skt*	*J1*	*5*

Signal Designation	Signal	Type	Description	Connector	Label	Pin
*+5V_iso *	*Input*	*DC*	*Isolated DC for Diff control lines*	*25D-type Plg*	*J2*	*13*
*+0V_iso *	*Input*	*DC*	*Isolated DC for Diff control lines*	*25D-type Plg*	*J2*	*1/25*
EXT_TRIGGER	Input	TTL Logic	Trigger	25D-type Plg	J2	2
Rtn	Input	Gnd		25D-type Plg	J2	14
BANK_SEL	Input	TTL Logic	(Bank Select) Chirp Direction	25D-type Plg	J2	3
Rtn	Input	Gnd		25D-type Plg	J2	15
EXT_CLOCK	Input	TTL Logic	External Data clock	25D-type Plg	J2	4
Rtn	Input	Gnd		25D-type Plg	J2	16
nc				25D-type Plg	J2	8
Mod4	Output	Logic	MOD_BIT4	25D-type Plg	J2	9
nc				25D-type Plg	J2	21
Mod1	Output	Logic	MOD_BIT1	25D-type Plg	J2	7
nc				25D-type Plg	J2	19
Mod2	Output	Logic	MOD_BIT2	25D-type Plg	J2	6
nc				25D-type Plg	J2	18
Mod3	Output	Logic	MOD_BIT3	25D-type Plg	J2	10
Mod_Rtn		Gnd		25D-type Plg	J2	22
MASTER_RST	Input	TTL Logic	Master Reset	25D-type Plg	J2	5
Rtn	Input	Gnd		25D-type Plg	J2	17
Norm/Prog_bit	Input	Switch	Pwr-ON Boot Strap Mode (BSL)	25D-type Plg	J2	11
Norm/Prog_bit_rtn	Input			25D-type Plg	J2	23
Auto/PC_bit	Input	Switch	Pwr-ON Command Option	25D-type Plg	J2	12
Auto/PC_bit_rtn	Input			25D-type Plg	J2	24
+12V (or +15V)	**Input**		**Supply**	**5-way 680 Plg (Binder)**	**J10**	**3**
0V	**Input**		**Supply RTN**	**5-way 680 Plg inder)**	**J10**	**4**
-12V (or -15V)	**Input**		**Supply**	**5-way 680 Plg (Binder)**	**J10**	**5**
+5V	**Input**		**Supply**	**5-way 680 Plg (Binder)**	**J10**	**1**
0V	**Input**		**Supply RTN**	**5-way 680 Plg (Binder)**	**J10**	**2**
AV_Freq	Output	0-10V Analog	Analog frequency	9D-type Plg	J3	1
AV_am	Output	0-10V Analog	Analog amplitude	9D-type Plg	J3	2
AV_rtn	Output	Rtn		9D-type Plg	J3	6
TestLASER_Bit	*Output*	*Logic*	*Laser Bit test signal*	*9D-type Plg*	*J3*	*5*
TestLASER_Bit_rtn				*9D-type Plg*	*J3*	*9*
FDATA (Chirp ctrl)	*I-O*	*Logic*	*Optional DDS control signal*	*9D-type Plg*	*J3*	*4*
Rtn				*9D-type Plg*	*J3*	*8*
SHAPE (Amp)	*Input*	*Logic*	*Optional DDS control signal*	*9D-type Plg*	*J3*	*3*
Rtn				*9D-type Plg*	*J3*	*7*

Note: *Greyed out* text indicates OEM options